Amplifier Design Challenges in 45nm CMOS Process, Within Low Voltage Supply and Digital Transistors Regime

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Agenda

• Why low voltage devices?
• Device’s operating regions and key role parameters.
• Low voltage Vs. 3.3V transistors.
• Techniques for increasing $r_o$ & $g_m$.
• Techniques for decreasing $V_{TH}$.
• Summary.
Low Voltage Transistors

We are dealing with 1.1V for the transistors, which can be exceeded to 1.25V maximum.

So why low voltage devices?

• Lower power consumption.
• Smaller area is needed for transistors with lower $L_{\text{min}}$.
• Long transistors slow down the performance.
Models for Analog Design

The following issues are the main concerns for Analog block’s design:

• Operation regions.
• Mutual conductance - $g_m$.
• Drain-Source resistance - $r_o$.
• Threshold voltage - $V_{TH}$.
• Device’s parasitic capacitances.
• Matching.
• Noise.

Since we are in digital process regime, some of the above mentioned parameters are not optimized for Analog design.
Operating Regions

We distinguish between the following operating regions:

**Cut-off**

\[ I_D = 0 \quad \text{for } |V_{GS}| < |V_{TH}| \]

**Linear (Ohmic)**

\[ I_D = K \left[ 2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2 \right] \quad \text{for } |V_{GS}| > |V_{TH}| \& |V_{GS} - V_{TH}| > |V_{DS}| \]

**Saturation**

\[ I_D = K \left( V_{GS} - V_{TH} \right)^2 \left( 1 + \lambda V_{DS} \right) \quad \text{for } |V_{GS}| > |V_{TH}| \& |V_{GS} - V_{TH}| < |V_{DS}| \]

\[ K = \frac{1}{2} \mu C_{OX} \frac{W}{L} \]

We can see that \((V_{GS} - V_{TH})\) and its relative value to \(V_{DS}\) has major influence on the transistor’s operation!
Small Signal Model

The equivalent small signal model for the MOS transistor is given in the figured below:

\[ g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \bigg|_{V_{DS}=\text{const}} = \frac{i_d}{v_{gs}} \bigg|_{v_{ds}=0} \]

\[ r'_o \equiv \frac{\partial V_{DS}}{\partial I_D} \bigg|_{V_{GS}=\text{const}} = \frac{v_{ds}}{i_d} \bigg|_{v_{gs}=0} \]

\[ g_{mb} \equiv \frac{\partial I_D}{\partial V_{BS}} \bigg|_{V_{DS}=\text{const}} = \frac{i_d}{v_{bs}} \bigg|_{v_{ds}=0} \]

We have major interest in 2 parameters, with the following expression for saturation region:

\[ g_m \approx 2\sqrt{KI_D} \]

\[ r'_o \approx \frac{1}{\lambda I_D} \]

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Transistor’s Intrinsic Gain

The following figure describes a basic amplifier. In saturation, the amplifier’s gain is given as follows:

\[ A_V \equiv \frac{v_{out}}{v_{in}} = -g_m r_o \frac{1}{1 + j \omega r_o C_L} \]

We can see that \( g_m \times r_o \) is the amplifier’s DC intrinsic gain!

What are typical values for \( g_m, r_o \) & \( V_{TH} \) for low voltage & 3.3V transistors?
### Typical Values

Some typical values for the transistor’s parameters:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LV NMOS</th>
<th>LV PMOS</th>
<th>3.3V NMOS</th>
<th>3.3V PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TH}$</td>
<td>460mV</td>
<td>-510mV</td>
<td>590mV</td>
<td>-580mV</td>
</tr>
<tr>
<td>$g_m$</td>
<td>1.5$m\Omega^{-1}$</td>
<td>1.1$m\Omega^{-1}$</td>
<td>1.4$m\Omega^{-1}$</td>
<td>1.1$m\Omega^{-1}$</td>
</tr>
<tr>
<td>$r_o$</td>
<td>15$K\Omega$</td>
<td>20$K\Omega$</td>
<td>115$K\Omega$</td>
<td>170$K\Omega$</td>
</tr>
<tr>
<td>$g_m \times r_o$</td>
<td>23</td>
<td>22</td>
<td>161</td>
<td>187</td>
</tr>
</tbody>
</table>

Though we have reduction in $V_{TH}$, $r_o$ is much reduced for the LV transistors!

We can see that the intrinsic gain of a single LV transistor is pretty low!

For example: implementation of 10bit Pipeline-ADC requires a 70dB amplifier, for the MSB stage.

We are interested in finding ways of increasing $g_m$ & $r_o$!
Increasing $r_o$ – Cascode

Let’s take a look at fully-differential architecture. At low frequency regime the gain would be:

$$A_v = \frac{v_{out} - v_{out}}{v_{in}} \approx g_{m1} r_{o1} \parallel r_{o3}$$

Using Cascode technique can much increase transistor’s $r_o$. A Reminder…

$$R_{out} = R + r_o + g_m r_o R \approx g_n r_o R$$

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Increasing \( r_o \) – Cascode (cont)

Applying the Cascode to the amplifier will result in the following architecture:

![Amplifier Circuit Diagram](image)

\[
A_v \equiv \frac{v_{out2} - v_{out1}}{v_{in1} - v_{in2}} \approx g_{m1} \left( g_{m3} r_o 3 r_o 1 \right) || \left( g_{m5} r_o 5 r_o 7 \right)
\]

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Increasing $r_o$ – Gain Boost

We can further increase the resistance using the gain-boost architecture:

$$R_{out} \approx A g_m r_o R$$

$$R_{out} \approx \left( g_m r_{o22} \parallel r_{o44} \right) g_m r_{o3} r_o$$
Applying the gain boost will result in the following architecture:

\[
A_v = \frac{v_{out2} - v_{out1}}{v_{in1} - v_{in2}} \approx Ag_{m1} \left( g_{m3}r_{o3}r_{o1} \right) || \left( g_{m5}r_{o5}r_{o7} \right)
\]

Increasing \( r_o \) – Gain Boost (cont)
Increasing $r_o$ – Large Lengths

$r_o$ is significantly increased by enlarging device’s length, so a significant intrinsic gain is obtained by increasing the length!

We may also improve other aspects by increasing device’s length:
1. Improving CMRR & PSRR.
2. Improving devices’ matching – proportional to $\left(\frac{W \times L}{2}\right)^{1/2}$.

On the other hand exaggerating in length increment, will results in slowness in performance!
Voltages’ Budget

To allow saturated transistors, $|V_{DS}|>150\text{mV}$ will be allocated for the transistors and with common mode voltage of $V_{COM}=500\text{mV}$:

We can see that $M_9$ is not well saturated $\rightarrow$ degradation in CMRR! Also this stacked architecture reduces the output swing.

This can be resolved by folded cascode architecture.
Folded cascode achieve higher output swing in the cost of power dissipation, gain and bandwidth!

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Voltage Boost

In switched-capacitor amplifier, voltage boost can be used to overcome the low $V_{GS}$ voltage:

\[ V_{DD} \quad V_{B2} \quad \phi \quad C \quad \overline{\phi} \quad V_{B1} \quad V_{REF} \]
Increasing $g_m$

We can increase $g_m$ by several ways:

1. **Increasing input stage (differential stage)** Drain current:  
   
   \[ g_m \propto \sqrt{I_D} . \]
   
   This will increase the power consumption and will reduce the intrinsic gain since:  
   
   \[ r_o \propto I_D^{-1} . \]

2. **Using double input stage (P & N devices).**
3. **Modulation of Bulk-Source voltage.**
Increasing $g_m$ – Double Input Stage
Increasing $g_m - V_{BS}$ Modulation

Modulation of $V_{BS}$ with input signal, will result in

$$g_{m,\text{eff}} = g_m + g_{mb},$$

where: $g_{mb} \propto \left(\beta + V_{SB}\right)^{-\frac{1}{2}}$
Decreasing $V_{TH}$

We saw that the value of $V_{TH}$ has a major influence on the transistor’s performance ($g_m$, $r_o$) and the saturation region. This is due to the fact that $V_{TH}$ is relatively high compared to the supply voltage. Decreasing $V_{TH}$ can contribute to circuit’s performance.

It can be decreased by the following ways:

1. Increasing device’s length.
2. Forward biasing of Bulk-Source junction.
3. Operating in sub-threshold.
Decreasing $V_{TH}$ – Increasing Length

$V_{TH}$ is decreased with enlarging device’s length:

We may also improve other aspects by increasing device’s length:
1. Improving CMRR & PSRR.
2. Improving devices’ matching – proportional to $\left(\frac{W \times L}{2}\right)^{\frac{1}{2}}$.

On the other hand exaggerating in length increment, will results in slowness in performance!
Decreasing $V_{TH} – BS$ Forward Biasing

For $V_{SB} \neq 0V$, $V_{TH}$ is decreased for negative values of $V_{SB}$, according to the following relation:

$$V_{TH} = V_{TH0} + \gamma \left( \sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right)$$

If we keep BS forward bias current low (<100pA), tens of mV can be reduced from $V_{TH}$!
“Decreasing” $V_{TH}$ – Sub-Threshold Operation

For $V_{GS} \approx V_{TH}$ the Drain current is exponentially dependent on the $V_{GS}$ voltage:

$$I_D = I_0 e^{\frac{V_{GS} - \zeta VT}{q}}$$

With typical values of $\zeta$, $V_{GS}$ decreases by ~80mV for $I_D$ to decrease by one decade.

In this case the intrinsic gain can reach close to one obtained in saturation region!

Though of possible instability of $I_D$ because of the exponential dependence on $V_{GS}$, sub-threshold region can be used for instance in the gain-boost amplifiers.
Summary

• Low voltage transistors have much smaller $r_o$, compared to 3.3V devices.
• The intrinsic gain of the transistor is too low to be simply used for common applications.
• Complex architectures should be used to gain back the mutual conductance, Drain-Source resistance and the intrinsic gain of the device.
• Operating in “non-conventional” regions can help to overcome the low intrinsic gain and relative high $V_{TH}$ voltage.
Thank you for your attention!