Insights into circuits for frequency synthesis at mm-waves

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Outline

- *Mm-wave applications, challenges of frequency synthesis*
- Inductor-less CMOS dividers operating at mmW
- Wide range low noise VCO in a scaled 32nm node
- Wideband receiver for Gbit/s communications
- Conclusions
From RF to mmW applications

- High data rate wireless communications
- Automotive radars
- Imaging (Security, Industrial controls, Medical diagnosis)
- Chemical sensors (spectrometers)

- Effort toward CMOS solution
  - High $f_T$, Integration with DSP, Low cost for large volumes
High data rate wireless communications

- ~7GHz of unlicensed bandwidth available around ~60GHz
- Intense standardization activity
  - WiGig, 802.11ad, WirelessHD, 802.15.3c, ECMA-387
Typical IF receiver at mm-waves

Frequency synthesizer is challenging: wide range and low noise at tens of GHz
Why low phase noise?

- Phase noise rotates signal constellation and impairs BER
- Phase noise <-113dBc/Hz @10MHz is required in most stringent cases, assuming 1MHz PLL bandwidth

Source: IEEE 802.15-06-0477-01-003c [Online]
Frequency Synthesizer

- Inductor-less CMOS dividers operating at mmW
- Wide-range low noise VCO in a 32nm scaled node
- Synthesizer for a receiver at Gbit/s
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For more, refer to:
A. Ghilioni et al., “mm-wave frequency dividers analysis and design based on dynamic latches with load modulation” to appear on JSSC
Injection locked dividers for mmW PLLs

- Limited power consumption
- Many examples demonstrated on bulk CMOS
- Limited tunability due to the LC resonance
- Large area due to the inductor
CML static dividers for mmW PLLs

- Very wide operating range
- Small area (no inductors)
- Large power consumption to reach mm-Waves
Differential pair as a dynamic CML latch

a) static

b) dynamic
c) dynamic, load modulated
Synchronous divider by four

Ring of four dynamic latches to perform frequency division by four
Waveforms assuming $R_{\text{Off}} \to \infty$

\[
\begin{align*}
V_p(t) &= V_{DD} - (V_{DD} - V_{p*}) e^{\frac{t-t_*}{R_{\text{on}}C_p}} \\
V_m(t) &= V_{m*} - (V_{m*} - V_{DD} + R_{\text{on}}I_b) \left(1 - e^{\frac{t-t_*}{R_{\text{on}}C_p}}\right)
\end{align*}
\]

When $V_p(t_1) - V_m(t_1) = V_{sw}$

\[
(t - t_*) = \frac{1}{2f_{\text{MAX}}}
\]
Maximum frequency of operation

\[ f_{\text{max}} = \frac{1}{2R_{\text{on}} C_p (1.41 + 0.59)^3} \]
Waveform with finite $R_{\text{off}}$

Rise time almost independent of $R_{\text{off}}$

$f_{\text{max}}$ starts reducing only assuming $R_{\text{off}} < 4R_{\text{on}}$

\[ R_{\text{on}} = 450 \Omega \]

\[ R_{\text{on}} = 635 \Omega \]
Impact of finite $R_{off}$ on $f_{min}$

To ensure locking, the voltage must not fall below $V_{sw}$ during the hold phases

\[ V_{DD} - \frac{t_{hold}}{R_{off} C_p} < V_{sw} \]

Capacitors’ discharge during hold phases determines a minimum operating frequency $f_{min}$.
Minimum frequency of operation

\[ f_{\min} = \frac{1}{2R_{\text{off}}C_p \ln(1/\gamma)} \]

\[ R_{\text{off}} = 4.5\, \text{k}\Omega \]
\[ R_{\text{off}} = 9\, \text{k}\Omega \]
Test chip photomicrograph

- Technology: 32nm bulk CMOS
- Core area: 18 x 55 μm²
- Supply voltage: 1V
Meas vs. sim: sensitivity curves
## Comparison with state of the art

<table>
<thead>
<tr>
<th>Ref</th>
<th>( f_{\text{in}/f_{\text{out}}} )</th>
<th>( f_{\text{min}} - f_{\text{max}} ) [GHz]</th>
<th>L.R. [%]</th>
<th>( P_{\text{diss}} ) [mW]</th>
<th>Area [( \mu m^2 )]</th>
<th>Tech CMOS [nm]</th>
<th>FoM [GHz(^2)/mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>3</td>
<td>58.6-67.2</td>
<td>13.7</td>
<td>5.2</td>
<td>170 x 220</td>
<td>65</td>
<td>111</td>
</tr>
<tr>
<td>[2]</td>
<td>3</td>
<td>48.8-54.6</td>
<td>3.5(^a)</td>
<td>3.0</td>
<td>300 x 300</td>
<td>65</td>
<td>31.0</td>
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<tr>
<td>[3]</td>
<td>4</td>
<td>79.7-81.6</td>
<td>2.4</td>
<td>12</td>
<td>106 x 330</td>
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<td>12.9</td>
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<td>4</td>
<td>62.9-71.6</td>
<td>3.2</td>
<td>2.8</td>
<td>110 x 130</td>
<td>90</td>
<td>58.7</td>
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<td>82.5-89.0</td>
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<td>3.0</td>
<td>220 x 290</td>
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<td>[6]</td>
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<td>67.0-72.4</td>
<td>7.7</td>
<td>15.5</td>
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<td>[7]</td>
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<td>58.5-72.9</td>
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<td>477</td>
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<tr>
<td>This work</td>
<td>4</td>
<td>14 – 70(^b)</td>
<td>60 – 90</td>
<td>1.3 – 4.8</td>
<td>18 x 55</td>
<td>32</td>
<td>471 – 581</td>
</tr>
</tbody>
</table>

\(^a\)Estimated from reported sensitivity curves.

\(^b\)Maximum input frequency limited by our available instrumentation.

FoM = \( \frac{\text{L.R.} \times f_{\text{max}}}{P_{\text{diss}}} \)
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For more, refer to:
E. Monaco et al., “A 33.6-to-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz minimum noise FOM using inductor splitting for tuning extension” ISSCC 2013
Issues of mmWave - VCOs

- Reduces dramatically with increasing oscillation frequency
- Wide tuning Range leads to poor phase noise FoM
- Achieving state of the art FoM and wide tuning range is challenging
Continuous scaling driven by complex Systems on Chip

~ 20-30% $f_T$ improvement only per generation

mmWave passive components penalty due to BEOL scaling
CMOS 65nm vs 32nm: BEOL

- 32nm H.L.M closer to substrate (~85%) but same thickness
- 32nm L.L.M. closer to substrate and thinner (~50%)
- 2 time resistivity of 32nm VIAs
Performance of MOS Switches

\[ r_{SW} \propto \frac{1}{g_M} \]

\[ c_{SW} \propto C_{GS} \]

- Trade-off between \( c_{SW} \) and \( r_{SW} \)
- \( FOM_{SW} \) measures quality of the switch:

\[ FOM_{SW} = c_{SW} \cdot r_{SW} \propto \frac{1}{f_T} \]
MOS Switch With Routing Parasitics

- Routing parasitics comparable to $r_{SW}$ and $c_{SW}$
- FOM tends to saturate in ultra scaled technologies
MOM capacitors realized with low level metals for max. density

MOM Q in 32nm ~70% than 65nm due to half thickness of Low Level of Metals and 2x via resistance
Switched Capacitor Structure

- Significant MOM loss ($R_{MOM}$) due to higher metals and vias resistivity. Much in the same way $C_{sw}$ limits tuning range

- Switched cap. tank does not benefit from technology scaling

$$Q_{low} = \frac{2}{\omega C_{MOM} (2R_{MOM} + r_{SW})}$$

$$\frac{C_{MAX}}{C_{MIN}} = \frac{C_{MOM}}{2c_{SW}} + 1$$
Q versus $C_{\text{MAX}}/C_{\text{MIN}}$

32nm switched MOM worse than 65nm

@40GHz
Inductors usually realized with top metals for maximum Q and self Resonance frequency

Slightly lower dielectric constant in 32nm compensates lower metal distance to substrate in 32nm
Switched Capacitor Oscillator

- \( C_{\text{FIX}} \): parasitic cap of buffer and core devices
- \( C_{\text{FIX}} \) equal or greater than \( C_T \) at mmW

- **SW ON:** \( f_{\text{MIN}} = \frac{1}{2\pi \sqrt{L_T (C_{\text{FIX}} + C_T)}} \)

- **SW OFF:** \( f_{\text{MAX}} \) determined by \( C_{\text{FIX}} \)

\[
f_{\text{MAX}} = \frac{1}{2\pi \sqrt{L_T \left( C_{\text{FIX}} + \frac{C_T c_{\text{SW}}}{C_T + c_{\text{SW}}} \right)}}
\]

\[
c_{\text{SW}} \ll C_T, C_{\text{FIX}} \rightarrow \frac{1}{2\pi \sqrt{L_T C_{\text{FIX}}}}
\]
Proposed Oscillator

- SW OFF: $C_{\text{FIX}}$ no more limiting $f_{\text{MAX}}$

- SW ON: $f_{\text{MIN}}$ as in switched cap. oscillator

$$f_{\text{MAX}} = \frac{1}{2\pi \sqrt{\frac{L_T}{C_T + C_{\text{FIX}} + c_{\text{SW}}}} \left(\frac{C_T + C_{\text{FIX}}}{C_T + C_{\text{FIX}} + c_{\text{SW}}} \right) c_{\text{SW}} \ll C_T, C_{\text{FIX}}}$$

- $c_{\text{SW}}$ in series with $C_T + C_{\text{FIX}}$

- Higher frequency jump
Comparison with same frequency jump

Assuming:  \( C_{\text{FIX}} = C_T = 100\text{fF}, \ L_T = 100\text{pF}, \ FOM_{\text{SW}} = 550\text{fs} \)
\( f_{\text{MIN}} = 35.6\text{GHz}, \ f_{\text{MAX}}/f_{\text{MIN}} = 1.2 \)

- \( c_{\text{SW}} = 50\text{fF} \)
- \( c_{\text{SW}} = 400\text{fF} \)

For the same frequency step, switch in the proposed tank may display much larger \( c_{\text{SW}} \)
Comparison with same frequency jump

Assuming: \( C_{\text{FIX}} = C_T = 100\text{fF}, \quad L_T = 100\text{pH}, \quad \text{FOM}_{SW} = 550\text{fs} \)
\( f_{\text{MIN}} = 35.6\text{GHz}, \quad f_{\text{MAX}} / f_{\text{MIN}} = 1.2 \)

\[
\begin{align*}
C_{\text{FIX}} & \quad C_T & \quad L_T \\
- r & \quad r_{SW} & \quad - r
\end{align*}
\]

\[
\begin{align*}
c_{SW} &= 50\text{fF} \\
r_{SW} &= 11\Omega \\
Q &= 8
\end{align*}
\]

\[
\begin{align*}
c_{SW} &= 400\text{fF} \\
r_{SW} &= 1.37\Omega \\
Q &= 16
\end{align*}
\]

Much lower \( r_{SW} \) leads to 2x tank \( Q \)
$Q \text{ vs } f_{\text{max}}/f_{\text{min}} \text{ with finite components } Q$

Advantage increase for higher frequency step and/or larger $C_{\text{fix}}$
Loop Gain with a conventional transconductor

\[ G_{LOOP} = g_M R_P \]

Switch ON \[ R_{PON} = \omega L_T Q_T \]

Switch OFF \[ R_{POFF} = \omega L_T Q_T \alpha^2 \]

\[ \alpha = \frac{c_{sw}}{C_T + C_{FIX} + c_{sw}} = 0.55 \div 0.75 \]

- Loop gain penalty
- Tank is an open at DC, latching issue
Loop Gain with Transformer Feedback

\[ G_{\text{LOOP}} = g_M Z_{21} \]

Switch ON

\[ Z_{21} = K \sqrt{\frac{L_S}{L_T R_{\text{PON}}}} \]

Switch OFF

\[ Z_{21} = K \sqrt{\frac{L_S}{L_T R_{\text{POFF}} \alpha}} \]

\[ \alpha = \frac{C_{sw}}{C_T + C_{\text{FIX}} + c_{sw}} = 0.55 \div 0.75 \]

• Transformer restores loop gain and avoids latching
Simulated Impedance $R_P$ and $Z_{21}$
Realized VCO

- Inductor splitting with $M_{SW}$ for largest tuning step
- Variable tank capacitance ($C_T$) with switched digital MOMs and varactor
- $L_T=100\text{pH}$, $C_T=140\text{fF}$, $C_{FIX}=120\text{fF}$
- Tank Q ranges from 4 to 5.5
- $R_b$ instead of PMOS mirrors lowers 1/f noise
Test Chip

- Direct output and after div. by 4 for Phase Noise measurement in X-Band (8-12GHz)
- CMOS 32nm LP from STMicroelectronics
- Supply voltage: 1V
- Core area: 70um x 120um
40GHz Phase Noise Measurement

**Graph:**
- **Y-axis:** Phase Noise [dBC/Hz]
- **X-axis:** Frequency Offset [Hz]
- The graph shows a trend line labeled $1/f^2$ and $1/f^3$, indicating the phase noise behavior across different frequency offsets.
Phase Noise and FoM over Tuning Range

- Phase Noise [dBc/Hz]
  - M\text{sw} ON
  - M\text{sw} OFF

- FOM [dBc/Hz]

Frequency [GHz]
### Summary and comparison

<table>
<thead>
<tr>
<th>REF</th>
<th>FREQ [GHz]</th>
<th>TR [%]</th>
<th>POWER [mW]</th>
<th>PN @10MHz [dBc/Hz]</th>
<th>FOM [dBc/Hz]</th>
<th>TECH</th>
</tr>
</thead>
<tbody>
<tr>
<td>[8]</td>
<td>57.5/90.1</td>
<td>44.2</td>
<td>8.4/10.8</td>
<td>-104.6/-112.2</td>
<td>172/180</td>
<td>65nm</td>
</tr>
<tr>
<td>[9]</td>
<td>11.5/22</td>
<td>59</td>
<td>20/29</td>
<td>-107/-127*</td>
<td>158.6/177.4</td>
<td>130nm</td>
</tr>
<tr>
<td>[10]</td>
<td>34.3/39.9</td>
<td>15</td>
<td>14.4</td>
<td>-118/-121*</td>
<td>178.4/180.1</td>
<td>65nm</td>
</tr>
<tr>
<td>[11]</td>
<td>43.2/51.8</td>
<td>22.9</td>
<td>16</td>
<td>-117/-119*</td>
<td>179/180</td>
<td>65nm</td>
</tr>
<tr>
<td>[12]</td>
<td>21.7/27.8</td>
<td>24.8</td>
<td>12.2</td>
<td>-121</td>
<td>177.5</td>
<td>45nm</td>
</tr>
<tr>
<td>This Work</td>
<td>33.6/46.2</td>
<td>31.6</td>
<td>9.8</td>
<td>-115.2/-118</td>
<td>177.5/180</td>
<td>32nm</td>
</tr>
</tbody>
</table>

* estimated from the reported phase noise at 1MHz
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For more refer to:
PHY for Gb/s wireless communications

- High Rate 60GHz PHY Proposal
- Large RF bandwidth (~9GHz minimum)
- RX Minimum Sensitivity: from -60dBm (1Gb/s) to -50dBm (4Gb/s)
- RX Maximum Noise Figure < 10dB
- Large LO tuning range required
- Very stringent phase noise at maximum data rate

RX architecture

- Sliding IF architecture

- First down-conversion to 1/3 of the received frequency
  - Only one PLL at 38.9 ÷ 43.2 GHz
  - Integrated PN: <-18dBc

- Injection Locked Dividers to generate I/Q IF signals
PLL architecture

Design strategy
- Increase CP current (2mA)
- *But* reduce VCO gain (500MHz/V)
- *And* optimize LPF to ensure stability

CP contribution to In-band phase noise:

\[ L_{CP} = \frac{S_{I_{cp}}}{2 \frac{I_{CP}}{2\pi} \frac{1}{N^2}} \]

Increasing \( I_{CP} \) reduces \( L_{CP} \) but stability becomes an issue
Phase noise measurements

- VCO Phase Noise: -118.5 dBc/Hz @10MHz from 40 GHz carrier
- Integrated Phase Noise: -22.5 dBc [10kHz-10MHz] from 60GHz carrier
mmW wideband receiver

- Technology: STM 65nm CMOS
- Area: 2.4mm²
- Power Consumption: 75mW
- Same Gain and Noise Figure
- VCO tuning range: 16%

![Diagram](image-url)
Comparison with state of the art

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Frequency tuning range [GHz]</td>
<td>37.3 - 43.9 (16.26%)</td>
<td>57 - 66 (14.6%)</td>
<td>17.5 - 20.94 (17.9%)</td>
<td>73.4 - 73.72 (0.4%)</td>
<td>59.6 - 64 (7.1%)</td>
</tr>
<tr>
<td>Phase noise at 10MHz offset [dBC/Hz]</td>
<td>-118.5 (41.76 GHz)</td>
<td>-99 (61.6 GHz)</td>
<td>-126 (20.88 GHz)</td>
<td>-108 (73.72 GHz)</td>
<td>-112 (60 GHz)</td>
</tr>
<tr>
<td>Equivalent phase noise at 10MHz from RF carrier [dBC/Hz]</td>
<td>-115 (62.64 GHz)</td>
<td>-99 (61.6 GHz)</td>
<td>-116.5 (62.64 GHz)</td>
<td>-109.8 (60 GHz)</td>
<td>-112 (60 GHz)</td>
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<tr>
<td>Integrated phase noise [dBC]</td>
<td>-22.5</td>
<td>N. A.</td>
<td>N. A.</td>
<td>N. A.</td>
<td>N. A.</td>
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<td>Power [mW]</td>
<td>33 + 11 (LO Buffer)</td>
<td>78</td>
<td>80</td>
<td>88**</td>
<td>26.3 + 15.4 (3 Buffers)</td>
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<td>1.1</td>
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<td>1.45</td>
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<td>45 CMOS</td>
<td>65 CMOS</td>
<td>90 CMOS</td>
<td>90 CMOS</td>
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</tbody>
</table>

* The supply voltage of PFD and CP is 1.8 V
** Without Output Buffer
Conclusions

- Several examples of realized mmW CMOS circuits for Local Oscillator generation have been presented.
- A wideband divider by-4 based on dynamic latches is attractive to replace traditional injection locked prescalers. Experiments show >60% fractional bandwidth, <5mw power, 55x18μm².
- VCO with >31% tuning range around 40GHz and a remarkable FOM from 177.5dBc/Hz to 180dBc/Hz despite being in an unfavorable ultra-scaled 32nm node.
- A 65nm PLL proves suitable to satisfy the stringent requirements of a wideband mmW receiver, exploiting the advantages of a sliding IF RX architecture.
References


References


References
