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EXPERIMENTAL MODEL AID FOR PLANAR DESIGN OF TRANSISTOR CHARACTERISTICS IN INTEGRATED CIRCUITS

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Abstract—A two-transistor lumped model is used to describe the main features of transistors' two dimensional action. The model provides a first order correction to the ideal one dimensional transistor gain due to the effect of the emitter periphery. The correction is given in terms of a single parameter which can be experimentally evaluated for a fixed diffusion process. This makes the model a practical tool in I.C. transistor layout design. Experimental virification of the model is presented. Finally, implication to gain and cutoff frequency falloff due to lateral injection at high current is suggested.

With the small planar dimensions used in today's monolithic integrated circuits and transistor production, the one-dimensional model does not describe faithfully enough the transistor action. To illustrate, observe that for a typical 2μ diffused 1×1 mil^2 emitter, the emitter periphery area is as much as one-third of the planar region area!

The influence of the emitter periphery on the transistor action should be examined carefully. Assuming that it draws emitter current proportional to its relative area[1] is oversimplification, and aggravates the periphery contribution. On the other hand, exact numerical solution of the two-dimensional transistor problem[2] requires repeated use of a computer for each case and is too elaborate for usual design purposes.

In standard integrated circuit production there is usually a fixed diffusion procedure which is used. Therefore all transistors have the same vertical doping parameters, especially if they appear in the same integrated circuit die. If these transistors could be considered as ideal one-dimensional devices, they would all have the same gain, cutoff frequency, and other parameters. In practice, transistors with different planar structure have somewhat different characteristics which are expected in view of the three-dimensional character of the device operation.

Because the diffusion procedure is fixed, we suggest that it may be possible and practical to use a simple model to describe the three-dimensional features of the transistor. The parameters of this model can be experimentally evaluated for a particular diffusion procedure by using a set of test transistors. These parameters can then be useful in planar design of transistors in integrated circuits, providing also some control on the transistor characteristics via its planar design.

A simplified model like this is described in Figs. 1 and 2, consisting of a two-transistor lumped model[3]. The real transistor is assumed to consist of two transistors connected in parallel; one is the planar region which is

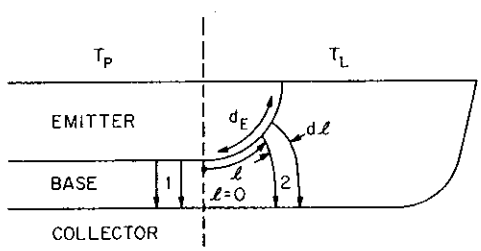

Fig. 1. Division of the transistor into planar and lateral regions.

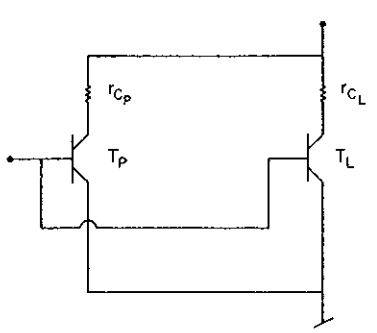

Fig. 2. The two-transistor lumped model.

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assumed to be an ideal one-dimensional transistor, and the other part is the low gain lateral region of the transistor.

We focus on calculating the gain of the lumped model of Fig. 2. We first calculate the common gain of two ideal n–p–n transistors with emitter area A_{E_1} and A_{E_2} when they are connected in parallel (Fig. 2). The hole and electron current densities are given by:

$$J_{Ep} = \frac{qn_i^2}{(Q_E/D_p)}(e^{qV_{EB}/kT} - 1) \tag{1}$$

$$J_{En} = \frac{qn_i^2}{(Q_B/D_n)}(e^{qV_{EB}/kT} - 1) \tag{2}$$

where

$$(Q_B/D_n) = \int_0^{W_B} \left(\frac{N_A(x)}{D_n}\right) dx \quad \text{and} \quad (Q_E/D_p) = \int_0^{L_p} \left(\frac{N_D(x)}{D_p}\right) dx$$

are the base and emitter factors. W_B is the base width and L_p the hole diffusion length into the emitter. The emitter factor (Q_E/D_p) is usually assumed to saturate at some constant value[4, 5].

We use eqns (1) and (2) to calculate the common gain of the two transistors. The common base gain of each transistor is determined by the emitter efficiency γ and the transport factor α_T: $\alpha = \gamma\alpha_T$. In terms of the α defect $\delta \equiv I_B/I_E = 1 - \alpha \simeq 1/\beta$ one gets[10]:

$$\delta = \frac{\delta_1 A_{E_1} + \delta_2 K A_{E_2}}{A_{E_1} + K A_{E_2}} \tag{3}$$

K is a parameter that determines the current distribution between the two transistors

$$K \equiv \frac{J_{E_2}}{J_{E_1}} \tag{4}$$

where J_{E_1} and J_{E_2} are the emitter current densities of the two transistors. The parameter K is voltage independent, since J_{E_2} and J_{E_1} have the same dependence on the common emitter-base voltage V_{BE} (eqns 1, 2).

In the limit $K(A_{E_2}/A_{E_1}) \ll 1$ a convenient linear relation results from first order expansion of eqn (3):

$$\delta = \delta_1 + (\delta_2 - \delta_1)K\frac{A_{E_2}}{A_{E_1}}. \tag{5}$$

Expression (5), with A_{E_1} being the planar transistor area, and A_{E_2} being the lateral transistor area, would be a very rough approximation to describe the two-dimensional operation. Since the current density across the lateral transistor varies considerably, a single parameter K (eqn 4) is not well defined. Extension of eqn (5) leads to:

$$\delta = \delta_p + \left[\int_0^{d_E} dl K(l)(\delta_L(l) - \delta_p)\right]\frac{L_E}{A_{E_p}} \tag{6}$$

where L_E is the emitter periphery length, d_E and l defined in Fig. 1, $\delta_L(l)$ is the alpha defect of the current tube which originates from point l (see Fig. 1) and

$$K(l) \equiv \frac{J_E(l)}{J_{EP}}. \tag{7}$$

The current injection into the lateral current tubes is much smaller than that injected into the planar part (see eqn 2), hence $K(l) \ll 1$. Either eqn (5) or eqn (6) can be generally written as:

$$\delta = \delta_p + \Delta_L \cdot \frac{L_E}{A_E} \tag{8}$$

where Δ_L is a constant parameter, uniquely determined for a given diffusion process.

At low current level there is significant contribution to gain reduction by recombination at the emitter-base junction space charge region, surface recombination, and emitter base channeling[1]. Still, a linear relation like eqn (6) follows straightforwardly for these cases too[10]. However, since the base currents which are contributed by these mechanisms have voltage dependence which is different from eqns (1) and (2), this leads the parameter Δ_L to be dependent on the emitter base voltage V_{BE}, so in evaluating Δ_L experimentally one must measure the gain of different transistors at the same emitter-base voltage, or roughly at the same current density.

We have prepared a set of photographic masks for fabrication of about 50 separately accessible test devices on a single die, including differently shaped bipolar transistors with different ratios of emitter periphery to area L_E/A_E. The test transistor array was diffused by standard two-step diffusion processes of boron and phosphorus into n type [100] plane silicon slices. The emitter base and base-collector vertical junction depths were $X_{EB} = 2\mu$ and $X_{BC} = 2{\cdot}7\mu$. The measured alpha defect (δ) of the different transistors was plotted vs L_E/A_E (Fig. 3). The linear relation (eqn 8) is reasonably satisfied. The small down deflection of point $L_E/A_E = 1{\cdot}33 \times 10^{-1}\mu^{-1}$ may be attributed to the second order term of the expansion of eqn 3 which carries a negative sign. The alpha defect values in Fig. 3 were calculated from the transistors maximum measured gain ($\delta = 1/\beta_{max}$) assum-

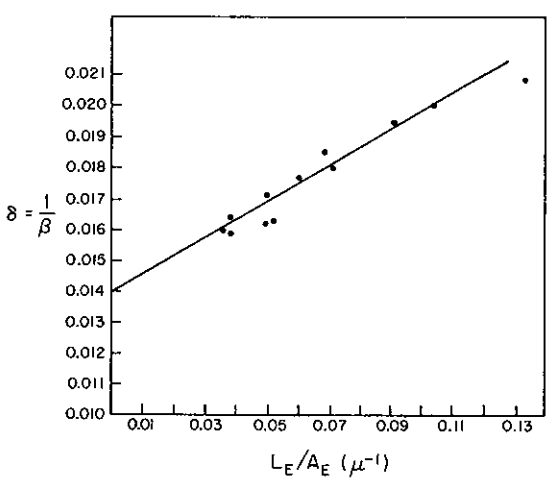

Fig. 3. α defect of different transistors located on the same chip vs their emitter periphery-to-area ratio.

ing that the maximum gain occurs at about the same current density in all transistors.

From the slope and the intersection of the ordinate axis (Fig. 3) we deduce the following model parameters which are valid for the particular process used: $\Delta_L = 5{\cdot}8 \times 10^{-2}\mu^{-1}$, $\delta_p = 0{\cdot}014$. The appropriate gain of the ideal planar transistor is $\beta = 1/\delta_p = 71{\cdot}5$.

The model suggested here is a simple first order correction to a one-dimensional model of the transistor [9]. We demonstrated in particular its use for the transistor gain calculation, however, we point out that some other parameters like cutoff frequencies and h_{FE} and f_T fall-off at high currents can also be investigated by this model, in conditions where these "fall offs" occur dominantly through the Van der Ziel mechanism [6].

Different mechanisms were suggested to explain the fall off of the mentioned transistor parameters at high currents [6, 7], and they apply at different transistor structures and different operating conditions. The mechanism that was suggested by van der Ziel *et al.* relates this fall off to the saturation of the planar part of the transistor at high currents, while the peripheral parts, normally carrying less current density, are not yet saturated. Recombination is higher and transit time is longer along the lateral transistor current tubes (see Fig. 1). Indeed these two effects are related through [9]

$$\frac{t_{tr}}{\tau} = 1 - \alpha_T = \delta_T. \tag{9}$$

where τ is the carrier's lifetime in the base. Since near saturation bigger portions of excess current will flow through the lateral parts, the overall small signal gain h_{FE} will fall (because of the reduced α_T) and the cutoff frequencies f_α, f_β and f_T will fall (because of increased t_{tr}). Hence we suggest that these effects can be also investigated [10] using the present simplified model of a single measurable parameter, which must be in this case voltage dependent $\Delta(V_{BE}, V_{CB})$. For a fixed I.C. diffusion process this may allow better control over these effects in the transistor's design, by varying the emitter periphery to area ratio, which determines the relative contribution of the peripheral transistor.

REFERENCES

1. C. A. Bittman, G. H. Wilson, R. J. Whittier and R. K. Waits, *IEEE J. Solid State Circuits* **SSC-5**, 29 (1970).
2. J. W. Slotboom, *Electron. Lett.* **5**, 677 (1969).
3. H. K. Gummel, *IEEE Trans. E. D.* **ED-11**, 455 (1964).
4. R. J. Whittier and J. P. Downing, International Electron Devices Meeting, Washington, D.C. 1968, Paper 12.4.
5. R. Berry, *Proc. IEEE* **57**, 1513 (1969).
6. A. van der Ziel and D. Azouvidis, *Proc. IEEE* **54**, 411 (1966).
7. R. J. Whittier, D. A. Tremere, *IEEE Trans. E. D.* **ED-16**, 39 (1969).
8. R. J. Whittier, *Solid St. Electron.* **13**, 61 (1970).
9. A. Gover, J. Grinberg, A. Seidman, *IEEE Trans. E. D.* **ED-19**, 967 (1972).
10. A. Gover, The Correlation between the Structure Parameters of Bipolar Transistors and Their Electrical Characteristics, M.S. Thesis, Tel Aviv University (1971).