Assignment No. 6

http://www.eng.tau.ac.il/~guy/Computer_Architecture/arch_home.html

In this exercise we would like to see whether the interrupt handling mechanism that we described in class is easily extendible to other types of interrupts.

For each of the following interrupts, discuss its properties (internal or external, repeat or continue, maskable, priority, etc.).

Discuss (in detail!) how it could be integrated into the mechanism (hardware support, data-path and control extensions).

1. Power supply crashes. Suppose we have a sensor that signals that the power supply is dying. When the event signal is activated there are about 30 ms before power will go down.

   Take into account the possibility of false alarm!

2. Memory protection violation. Suppose that there are registers in the architecture, the contents of which are set by the operating system. These registers define the range of memory addresses that the process may access.

   When a process attempts to access an address out of this legal range, an interrupt occurs.

3. Hardware failures. Consider a bus with an error detection code (for example, a parity bit). If an error is detected, an event signal is activated. Consider two cases: (a) error is not fatal, but a re-transmit is required; and (b) error is fatal, or re-transmit does not help.

4. Breakpoint. Suppose that there is a register that holds an address, a, such that when $PC = a$, the program should stop (not abort), and pass control to another program (a debugger).

5. Tracing. Suppose that the programmer wishes to have a file that holds the list of instructions that were executed during a program execution. (Should tracing effect in any way program execution? does it?)