Dr. Guy Even
Dept. of Electrical Engineering – Systems
Tel–Aviv University
Class: Thursdays 16-18, Wolfson-Kitot 102
Non-formal exercise: Thursdays 18-19, Wolfson-Kitot 102

General

The course will attempt to deal with concrete issues in computer architecture. We will study, step by step, various enhancements of a simple RISC architecture. Implementation, cost, and delay of each step will be discussed.

Topics

- A simple (without cache, no pipelining) RISC Machine (DLX).
- Support of precise interrupts on a DLX Machine.
- Memory system design: memory hierarchy, caches.
- Pipelining of a DLX Machine. We will also discuss the effect of pipelining on supporting precise interrupts.
- Instruction level parallelism and scheduling mechanisms for out-of-order execution. Two mechanisms will be studies: Scoreboard and the Tomasulo Algorithm.
- More topics, as time permits: Floating Point Units, Virtual Memory, etc.

Grade

There will be a final exam in this course which will determine the final grade.

Exercises

Homework assignments will be given and will be discussed in the non-formal exercises. It is expected that the students will do most of the talking during the non-formal exercises.

References

Henessy & Patterson, Computer Architecture: A Quantitative Approach.
Muller & Paul, The complexity of Simple Computer Architectures.
and various papers (details later).