Chapter 1: The digital abstraction

Computer Structure
&
Intro. to Digital Computers

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Digital Circuits vs. Analog Devices

Property	Digital Circuit	Analog Device
values	$\{0,1\}$	$\mathbb{R}$
description	simple (Boolean function)	complicated (differential eq.)
real?	abstract model	very real

Conclusion: much easier to use the digital abstraction than the realistic, complete, complicated analog model.

Preliminary questions

- what is an analog device? (components, behavior)
- in what way does a digital circuit model an analog device?
  - can every analog device be modeled as a digital circuit?
  - what type of digital circuits do we want?
  - why is one inverter better than another?
- how can we tell if an analog device is a gate (say, an inverter)?

Transistors

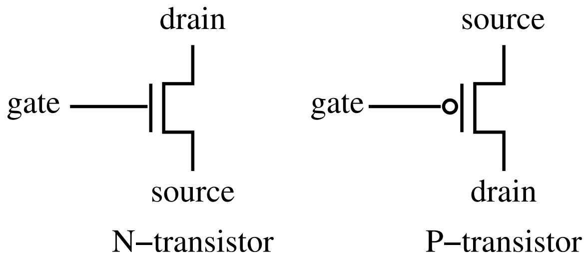
Computers $\Rightarrow$ VLSI chips $\Rightarrow$ gates & flip-flops $\Rightarrow$ transistors
Transistors are the basic components.
Most common VLSI technology is called CMOS.
In CMOS: only two types of transistors:

- N-transistor
- P-transistor

in case you are curious:
VLSI = Very Large Scale Integration

CMOS = Complementary Metal-Oxide Semiconductor

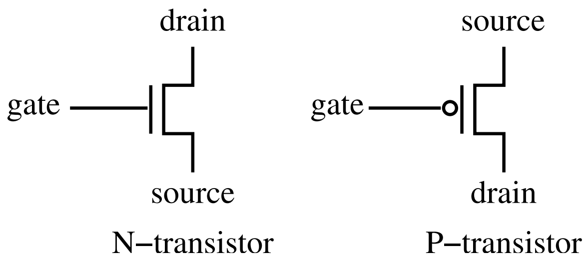
N-transistor & P-transistor



Inputs: gate & source
Output: drain

(not accurate! just for the sake of this discussion)

N-transistor & P-transistor



Functionality of N-transistor:

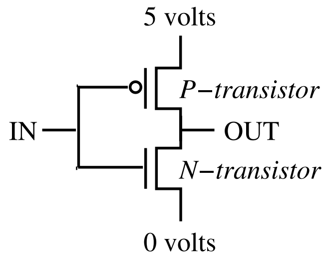
- If $v(gate) = high$, then $resistance(source, drain) = 0$ (and then $v(drain) \leftarrow v(source)$)
- If $v(gate) = low$, then $resistance(source, drain) = \infty$

Functionality of P-transistor:

- If $v(gate) = high$, then $resistance(source, drain) = \infty$
- If $v(gate) = low$, then $resistance(source, drain) = 0$

Story true if: $v(s) = high$ in P & $v(s) = low$ in N.

A CMOS inverter



IN $= low$**:**

- P-transistor is conducting
- N-transistor is not conducting

$\Rightarrow v(OUT) = high$

IN $= high$**:**

- P-transistor is not conducting
- N-transistor is conducting

$\Rightarrow v(OUT) = low$

Qualitative Analysis vs. Quantitative Analysis

Qualitative analysis:

- gives an idea about "how an inverter works".
- no idea about actual voltages of output as a function input voltage.
- no idea about how long it takes the output to stabilize.

Quantitative analysis:

- based on precise modeling of transistor.
- computes precise input-output relationship.
- requires a lot of work (usually done with the aid of a computer program called SPICE).

Analog signals

An analog signal is a real function

$$f : \mathbb{R} \rightarrow \mathbb{R},$$

where $f(t) =$ voltage as a function of the time.

Assumption: wires have zero resistance, zero capacity, and signals propagate through wires without delay.
$\Rightarrow$ voltage along a wire is identical at all times.

Since a signal describes the voltage (i.e. derivative of energy as a function of charge), we also assume that a signal is a continuous function.

Digital signals

A digital signal is a function

$$g : \mathbb{R} \rightarrow \{0, 1, \text{non-logical}\}.$$

The value of a digital signal describes the logical value carried along a wire as a function of time.

- zero & one : logical values.
- non-logical: indicates that the signal is not digital.

Interpreting analog signals as digital signals

Q: How does one interpret an analog signal as a digital signal?

naive answer: define a threshold voltage V'.
Consider an analog signal $f(t)$.

The digital signal *dig*$(f(t))$ is defined as follows.

$$\textit{dig}(f(t)) \triangleq \begin{cases} 0 & \text{if } f(t) < V' \\ 1 & \text{if } f(t) > V' \end{cases}$$

Q: is this a useful definition?

problems with definition of *dig*$(f(t))$

- All devices in a circuit must use exactly the same threshold V'. This is impossible due to manufacturing tolerances.
- Perturbations of $f(t)$ around V' lead to unexpected values of *dig*$(f(t))$.
  example: measure weight w using a spring. Wish to compare of length ℓ of spring with ℓ_t. Spring length oscillates around ℓ. If $\ell \approx \ell_t$, then comparison requires a long time.

$\Rightarrow$ must separate thresholds for 0 and for 1.

Interpreting analog signals as digital signals

Q: How does one interpret an analog signal as a digital signal?

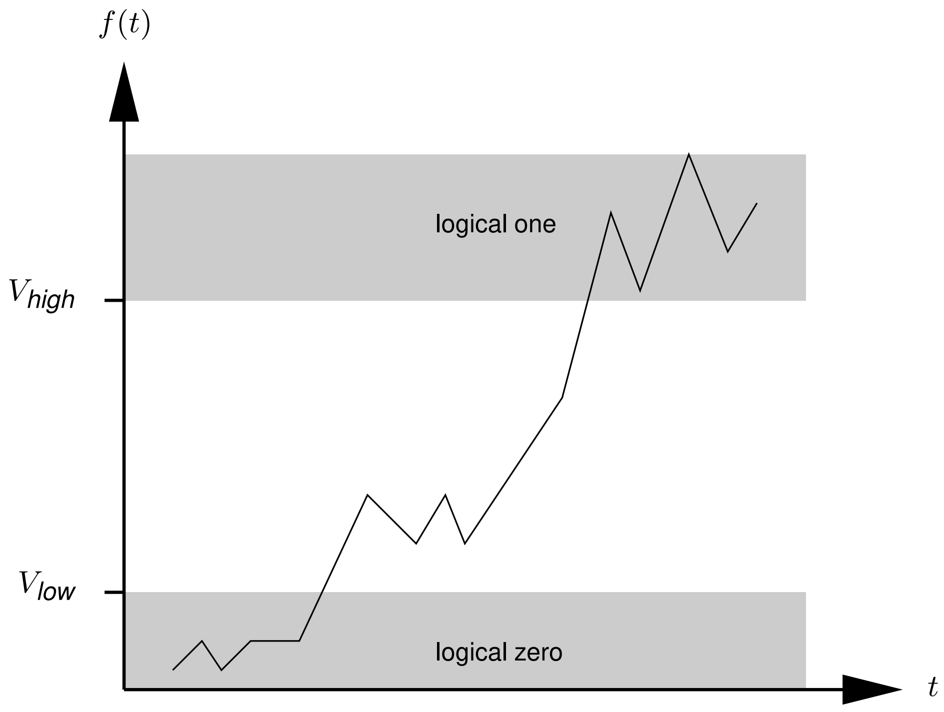
A: Two voltage thresholds are defined: $V_{low} < V_{high}$.

Consider an analog signal $f(t)$.

The digital signal *dig*$(f(t))$ is defined as follows.

$$\textit{dig}(f(t)) \triangleq \begin{cases} 0 & \text{if } f(t) < V_{low} \\ 1 & \text{if } f(t) > V_{high} \\ \text{non-logical} & \text{otherwise.} \end{cases}$$

digital interpretation of an analog signal



did we solve the problems of a single threshold?

- manufacturing requirements: a low output must be $\leq V_{low}$ & a high output must be $\geq V_{high}$.
- fluctuations of $f(t)$ around V_{low} still cause fluctuations of *dig*$(f(t))$.
  However, these fluctuations are between 0 and "non-logical" (not between 0 and 1). This is still a problem, but not as bad...

Will noise cause a problem?

Noise = undesired changes to $f(t)$. Back to the example of a weight hanging from a spring: wind causes changes in the spring length and disturbs measurement of spring length.

An inverter

Q: define an inverter.

A:

$$\textit{dig}(OUT(t)) \triangleq \begin{cases} 0 & \text{if } \textit{dig}(IN(t)) = 1 \\ 1 & \text{if } \textit{dig}(IN(t)) = 0 \\ \text{non-logical} & \text{otherwise.} \end{cases}$$

We will see shortly that: noise $\Rightarrow$ cannot use these definitions to build correct circuits.

Before we can answer that we need to discuss transfer functions...

Transfer functions

The voltage at an output of a gate depends on the voltages of the inputs of the gate. This dependence is called the transfer function.

Example: an inverter with an input x and an output y. The value of the signal $y(t')$ at time t' is a function of the signal $x(t)$ in the interval $(-\infty, t']$.

Static transfer function: if the input $x(t)$ is stable for a sufficiently long period of time and equals x_0, then the output $y(t)$ stabilizes on a value y_0 that is a function of x_0.

If this were not the case, then we have a memory device not a logical gate.

Static transfer function

Let G denote a gate with one input x and one output y.

Definition: A function $f : \mathbb{R} \to \mathbb{R}$ is a static transfer function of a gate G if

$$\exists \Delta > 0 \ \ \forall x_0 \ \ \forall t_0 \ : \qquad \forall t \in [t_0 - \Delta, t_0] \ \ x(t) = x_0 \quad \Longrightarrow \quad y(t_0) = f(x_0).$$

- Δ - propagation delay (time required for stable output)
- x_0 - stable input voltage
- t_0 - time in which $y(t)$ is measured

Static transfer function - remarks

(1) Since circuits operate over a bounded range of voltages, static transfer functions are usually only defined over bounded domains and ranges (say $[0, 5]$ volts).

Static transfer function - remarks

(2) Allow perturbations of $x(t)$ and $y(t)$.

$$\forall \epsilon \;\; \exists \delta, \Delta > 0 \;\; \forall x_0, t_1, t_2 \;\; :$$
$$\forall t \in [t_1, t_2] \;\; : \;\; |x(t) - x_0| \leq \delta$$
$$\Longrightarrow$$
$$\forall t \in [t_1 + \Delta, t_2] \;\; : \;\; |y(t) - f(x_0)| \leq \epsilon.$$

- δ - measures stability of input $x(t)$
- ϵ - measures stability of output $y(t)$
- $[t_1, t_2]$ - interval during which $x(t)$ is ϵ-stable.
- $[t_1 + \Delta, t_2]$ - interval during which $y(t)$ is δ-stable.

Propagation delay Δ depends only on ϵ (which is fixed and the same for all gates).

back to the definition of an inverter

$$dig(OUT(t)) \triangleq \begin{cases} 0 & \text{if } dig(IN(t)) = 1 \\ 1 & \text{if } dig(IN(t)) = 0 \\ \text{non-logical} & \text{otherwise.} \end{cases}$$

or equivalently,

$$IN(t) < V_{low} \Longrightarrow OUT(t) > V_{high}$$
$$IN(t) > V_{high} \Longrightarrow OUT(t) < V_{low}$$

Q: Define a NAND-gate.

Noise

$$A \xrightarrow[\hspace{6cm}]{\textit{wire}} B$$

Noise signal: the difference $B(t) - A(t)$. (reference signal = $A(t)$).

Q: what causes noise?

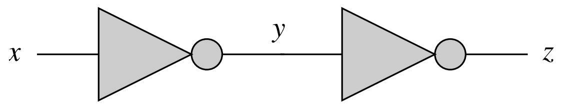
A: The main source of noise is heat. Heat causes random movement of electrons. These random movements do not cancel out perfectly, and random currents are created. These random currents create perturbations in the voltage of a wire.

Bounded noise model

- Bounded noise model - the noise signal along every wire has a bounded absolute value.
- Uniform bounded noise model - $\exists \epsilon > 0$ such that the absolute value of all noise signals is bounded by ϵ.
- Justification - noise is a random variable whose distribution has a rapidly diminishing tail. If the ϵ is sufficiently large, then

$$Prob[|\text{noise}| > \epsilon] \approx 0.$$

The digital abstraction in the presence of noise



Assume that:

- $x > V_{high}$, so *dig*$(x) = 1$,
- $y = V_{low} - \epsilon'$, for a very small $\epsilon' > 0$.
- $\Rightarrow dig(z) = 1$.

What if input to 2nd inverter equals $y(t) + n_y(t)$?

If $n_y(t) > \epsilon$, then *dig*(y) = non-logical, and can't deduce that $dig(z) = 1$.

$\Rightarrow$ must strengthen the digital abstraction!

Redefining the digital interpretation of analog signals

Deal with noise: interpret input signals and output signals differently.

Input Signal: a signal measured at an input of a gate.

Output Signal: a signal measured at an output of a gate.

Redefining the digital interpretation (cont.)

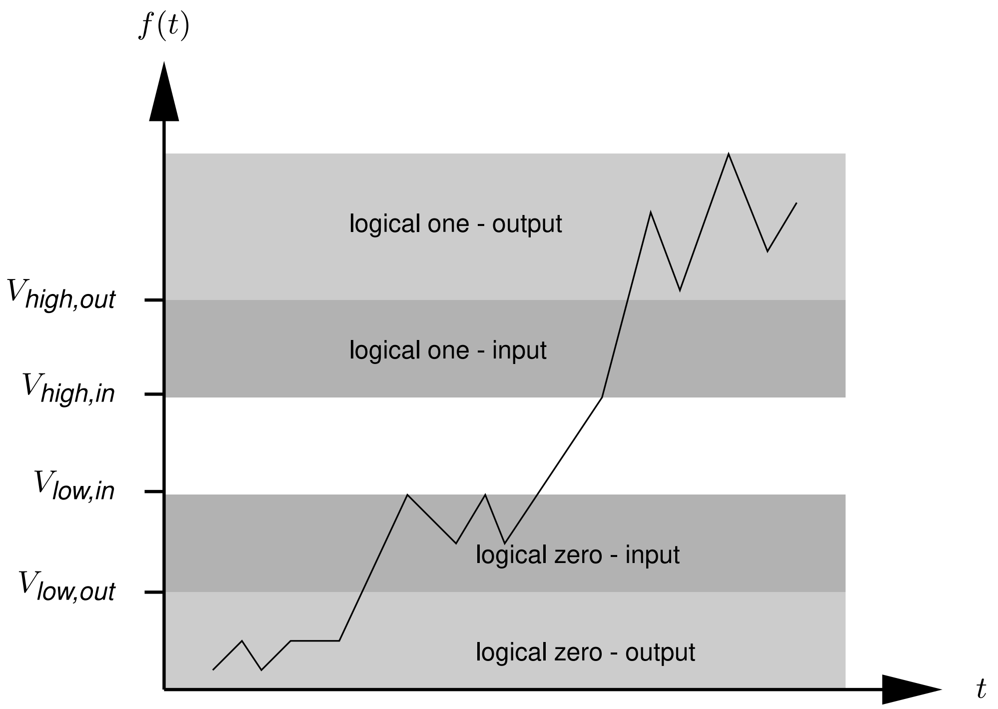
Instead of two thresholds, V_{low} and V_{high}, we define the following four thresholds:

- $V_{low,in}$ - an upper bound on a voltage of an input signal interpreted as a logical zero.
- $V_{low,out}$ - an upper bound on a voltage of an output signal interpreted as a logical zero.
- $V_{high,in}$ - a lower bound on a voltage of an input signal interpreted as a logical one.
- $V_{high,out}$ - a lower bound on a voltage of an output signal interpreted as a logical one.

These four thresholds satisfy the following equation:

$$V_{low,out} < V_{low,in} < V_{high,in} < V_{high,out}.$$

Redefining the digital interpretation (cont.)



Digital interpretation of input & output signals

Consider an input signal $f_{in}(t)$. The digital signal $dig(f_{in}(t))$ is defined as follows.

$$dig(f_{in}(t)) \triangleq \begin{cases} 0 & \text{if } f_{in}(t) < V_{low,in} \\ 1 & \text{if } f_{in}(t) > V_{high,in} \\ \text{non-logical} & \text{otherwise.} \end{cases}$$

Consider an output signal $f_{out}(t)$. The digital signal $dig(f_{out}(t))$ is defined analogously.

$$dig(f_{out}(t)) \triangleq \begin{cases} 0 & \text{if } f_{out}(t) < V_{low,out} \\ 1 & \text{if } f_{out}(t) > V_{high,out} \\ \text{non-logical} & \text{otherwise.} \end{cases}$$

Noise margins

The differences

$$V_{\textit{low,in}} - V_{\textit{low,out}} \quad \text{and} \quad V_{\textit{high,out}} - V_{\textit{high,in}}$$

are called noise margins.

Claim: If the absolute value of the noise is less than the noise margin, then the logical value of an output signal is unchanged.

Proof: If the absolute value of the noise $n(t)$ is bounded by the noise margins, then an output signal $f_{out}(t) < V_{\textit{low,out}}$ will result with an input signal $f_{in}(t) = f_{out}(t) + n(t) < V_{\textit{low,in}}$. $\square$

Inverter - revisited

We are now ready to define an inverter.

Definition: Let G denote a device with one input x and one output y. The device G is an inverter if its static transfer function $f(x)$ satisfies:

$$x(t) < V_{\textit{low,in}} \Longrightarrow y(t) > V_{\textit{high,out}}$$
$$x(t) > V_{\textit{high,in}} \Longrightarrow y(t) < V_{\textit{low,out}}.$$

Q: can you define a NAND-gate?

Logical & stable analog signals

back to the zero-noise model (to simplify the discussion)...

logical signal: $f(t)$ is logical at time t if *dig*$(f(t)) \in \{0,1\}$.

stable signal: $f(t)$ is stable during the interval $[t_1, t_2]$ if $f(t)$ is logical for every $t \in [t_1, t_2]$.

Claim: If an analog signal $f(t)$ is stable during the interval $[t_1, t_2]$ then one of the following holds:

1. *dig*$(f(t)) = 0$, for every $t \in [t_1, t_2]$, or
2. *dig*$(f(t)) = 1$, for every $t \in [t_1, t_2]$.

Proof: Continuity of $f(t)$ & $V_{low} < V_{high}$. □

Logical & stable digital signals

Let $x(t)$ denote a digital signal.

logical signal: $x(t)$ is logical at time t if $x(t) \in \{0,1\}$.

stable signal: $x(t)$ is stable during the interval $[t_1, t_2]$ if $x(t)$ is logical for every $t \in [t_1, t_2]$.

Summary

- Signals - analog & digital
- Noise - bounded noise model & zero noise model
- Digital interpretation of analog signals
- Transfer functions
- Definition of gate (e.g. inverter) using transfer function
- Stable & logical signals