Chapter 11: Additional Components

Computer Structure & Intro. to Digital Computers

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Goals

- define drivers (3-state buffers).
- define Read Only Memory (ROM).
- define Random Access Memory (RAM).

Drivers

DEF: A driver is a device defined as follows:

Input: IN, *enable* $\in \{0, 1\}$.

Output: $OUT \in \{0, 1\}$.

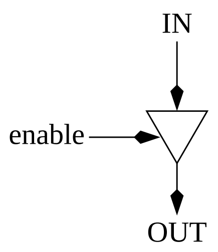
Functionality:

$$OUT = \begin{cases} IN & \text{if } \textit{enable} = 1 \\ \text{not-connected} & \text{otherwise.} \end{cases}$$

Remark:

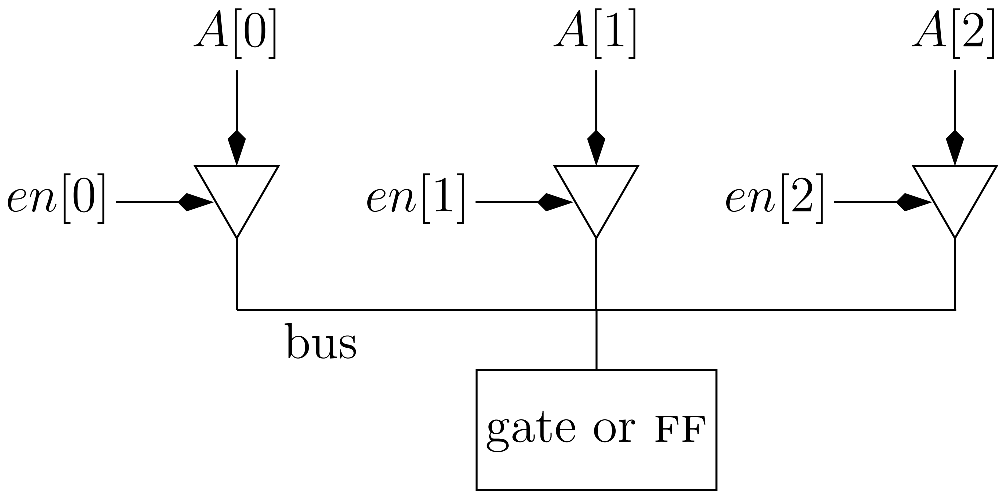
- A driver is not a combinational circuit.
- A driver is in one of two “states”:
  - connected - a “wire” between IN and OUT.
  - disconnected - value of IN does not affect value of OUT.

Drivers - cont.

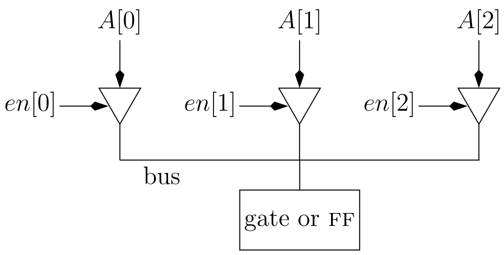


Remark: technology dependent: when connected either uni-directional or bi-directional. (can always force uni-directional by connecting two inverters in series to OUT.)

Bus fed by drivers



Bus fed by drivers - cont



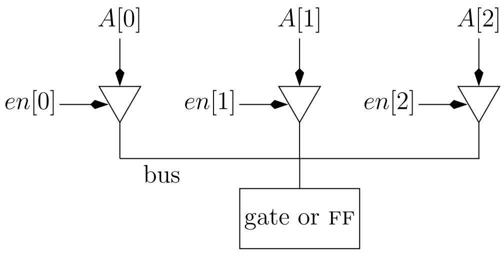
Design rule: If net N is fed by a driver, then every component feeding N must be a driver.

Semantic rule: stable values of $en[0], \ldots, en[k-1]$ satisfy:

$$\sum_{i=0}^{k-1} en[i] = 1.$$

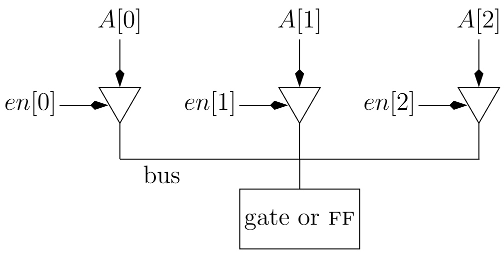
Why use driver fed buses?

- Could use $k:1$-MUX instead.
- Driver fed bus is simpler in a "distributed" situation:
  - Signals $A[i]$ are computes in different locations, single wire connecting these locations carries the selected signal.
  - Still need to connect separate wires for $en[i]$.



Disadvantage of driver fed buses?

- If sematic rule is violated $\sum_{i=0}^{k-1} en[i] > 1$, then conflicting drivers can damage the circuit.
- $\Rightarrow$ no drivers in lab work.



Read Only Memory (ROM)

two parameters:

- a - $A = 2^a$ number of memory "words" .
- d - number bits per memory word.

DEF: A ROM(a, d) is a combinational circuit defined as follows:

Input: *Address* $\in \{0,1\}^a$.

Output: $D \in \{0,1\}^d$.

Functionality:

$$D = M[\langle \textit{Address} \rangle],$$

$M[0..(A-1)]$ is a vector of binary strings $\in \{0,1\}^d$.

Remark: ROM(a, d) stores the vector $M[0..(A-1)]$, and outputs $M[\langle \textit{Address} \rangle]$.

ROM

- A ROM(a, d) implements a boolean function

$$f : \{0,1\}^a \rightarrow \{0,1\}^d.$$

- ROM(a, d) is loaded with the contents of vector $M[0..(A-1)]$ during fabrication.
- Other technologies enable loading of ROM after fabrication or even on-board (EPROM,EEPROM, flash memory).

Random Access Memory (RAM)

- Abstract: stores a vector $M[0..A-1]$ of words.
- Allows reading the contents of vector entry:

$$D_{\text{out}} \leftarrow M[\langle \textit{Address} \rangle].$$

- Allows writing contents into a vector entry:

$$M[\langle \textit{Address} \rangle] \leftarrow D_{\text{in}}.$$

- Complicated devices (not combinational and not synchronous) - designed to be as efficient as possible.
- Communication with external world according to a bus protocol.
- S-RAM slides

RAM as main memory of a processor

- Communication between processor and RAM is done via dedicated registers (MAR, MDR) and by a bus.
- One often puts controllers (FSMs) that controll the bus signals and inform processor when memory access is completed.
- Bus protocol and controller - topic of lab work next semester.