Introduction to Digital Computers - Spring 2000

Assignment No. 4

Course homepage: http://www.eng.tau.ac.il/~guy/Digital_Computers00/

Firm Deadline: March 30th - before the beginning of the lecture

1. A cyclic shift (to the left) by one position is the function $c^1 : \{0,1\}^n \to \{0,1\}^n$ defined by

$$c^1(a[n-1:0]) = a[n-2:0] \cdot a[n-1].$$

A cyclic shift by $i+1$ positions is defined recursively by:

$$c^{i+1}(a[n-1:0]) = c^1(c^i(a[n-1:0])).$$

   (a) Design a circuit $CLS(n,i)$ (cycle left shift by i positions) defined as follows:

   input: $a \in \{0,1\}^n$ and $s \in \{0,1\}$.

   output: $x \in \{0,1\}^n$ defined by

$$x[n-1:0] = \begin{cases} a[n-1:0] & \text{if } s=0 \\ c^i(a[n-1:0]) & \text{if } s=1 \end{cases}$$

   What is the cost and delay of your design? (Do not apply i successive shifts.)

   (b) Design a cyclic shifter $CLS(n)$ defined as follows:

   input: $a \in \{0,1\}^n$ - the string to be shifted. $b \in \{0,1\}^{\lceil \log_2 n \rceil}$ - the shift amount.

   output: $c^{\langle b \rangle}(a[n-1:0])$.

   hint: Use $CLS(n,2^i)$ for $i = 0,1,\ldots,k$ (where $k = \lceil \log_2 n \rceil - 1$).

   (c) Prove the correctness of your design.

   (d) Analyze the cost and delay of your $CLS(n)$ design.

2. A bi-directional cyclic shift can be either to the left or to the right. We denote a right shift by one position as a left shift by (-1) positions, as follows:

$$c^{-1}(a[n-1]:0) = a[0] \cdot a[n-1:1].$$

A cyclic right shift by $i+1$ positions is defined by:

$$c^{-(i+1)}(a[n-1:0]) = c^{-1}(c^{-i}(a[n-1:0])).$$

   (a) Prove that if $x = y \pmod{n}$, then

$$c^x(a[n-1:0]) = c^y(a[n-1:0])$$

   (b) Prove that if $s \in \{0,1\}^m$ and $n = 2^m$, then

$$c^{[s[m-1:0]]}(a[n-1:0]) = c^{\langle s[m-1:0] \rangle}(a[n-1:0])$$

(c) Design a bi-directional cyclic shifter $BiCLS(n)$ defined as follows:

input: Assume $n = 2^m$. Let $a \in \{0,1\}^n$ - the string to be shifted and $b \in \{0,1\}^m$ - the shift amount.

output: $c^{[b[m-1:0]]}(a[n-1:0])$.

(d) Prove the correctness of your design.

(e) Analyze the cost and delay of your $BiCLS(n)$ design.

(f) Consider a processor that has two types of cyclic shift instructions: "shift left by $\langle s \rangle$ positions" and "shift right by $\langle s \rangle$ positions". Assume $n = 2^m$ (length of string to be shifted). Suggest an implementation for these shifts. Assume that the shift amount is represented as a binary number and that the shift direction is given by a bit. Can you do better than design two separate cyclic shifters? Can you avoid the delay of the increment in the conversion of binary numbers to 2's complement representation?

3. Draw the $PPC(16)$ circuit using only $*$-gates (that is, unfold the recursion). What is the fanout of $PPC(n)$?

4. The description of $CLA(n)$ given in class did not address the issue of how the alphabet $\{0,1,2\}$ is encoded. Three encodings are given in the Table below:

symbol	binary encoding	"hot one" encoding	"g & p" encoding
0	00	001	00
1	01	010	01
2	10	100	10 or 11

(a) For every encoding: design a $*$-gate, design the computation of $\sigma[i] = a[i] + b[i]$, and design the computation of the carry-bits from $\pi[i]$.

(b) Compute the cost and delay of $CLA(n)$ with respect to each encoding according to the Motorola technology for $n = 8, 16, 32, 64, 128$.

(c) Modify the $PPC(n)$ design so that the fanout is 2. Use 1-buffers to limit the fanout of $PPC(n)$ to 2. How does this modification change the asymptotic growth of the cost and delay? Re-compute the cost and delay of $CLA(n)$ for the same values of n.