Introduction to Digital Computers - Spring 2000
Assignment No. 5
Course homepage: http://www.eng.tau.ac.il/~guy/Digital_Computers00/

Firm Deadline: April 11th - before the beginning of the lecture

1. What does a two's complement adder output when an overflow occurs? Let:
   - $a[n-1:0], b[n-1:0] \in \{0,1\}^n$; and
   - $z = [a[n-1:0]] + [b[n-1:0]]$.

   Suppose that
   $$\langle c[n] \cdot s[n-1:0] \rangle = \langle a[n-1:0] \rangle + \langle b[n-1:0] \rangle.$$
   Prove that:

   (a)
   $$[s[n-1:0]] = z \pmod{2^n}$$

   (b) Suppose that $z \notin T_n$ and that $z > 0$. Write the smallest interval that z belongs to. Write a closed formula for $[s[n-1:0]]$. What is the interval that $[s[n-1:0]]$ belongs to?

   (c) Suppose that $z \notin T_n$ and that $z < 0$. Write the smallest interval that z belongs to. Write a closed formula for $[s[n-1:0]]$. What is the interval that $[s[n-1:0]]$ belongs to?

   (d) Write and execute a C program that demonstrates your answers. Clue: a and b are added as unsigned and stored in an unsigned variable s. Print a, b, and s as signed integers. (You may use another programming language if you like.)

2. Unsigned subtraction. Let:
   - $a[n-1:0], b[n-1:0] \in \{0,1\}^n$; and
   - $z = \langle a[n-1:0] \rangle - \langle b[n-1:0] \rangle$

   Suppose that
   $$\langle c[n] \cdot s[n-1:0] \rangle = \langle a[n-1:0] \rangle + \langle \overline{b[n-1:0]} \rangle + 1.$$
   Answer the same questions asked for addition for this case.

3. Let $\langle c[n] \cdot s[n-1:0] \rangle = \langle a[n-1:0] \rangle + \langle b[n-1:0] \rangle$. We know that an overflow occurs in two's complement addition if and only if $c[n] \neq c[n-1]$. Prove that
   $$c[n] \neq c[n-1] \text{ iff } (a[n-1] = b[n-1]) \text{ and } (a[n-1] \neq s[n-1])$$

4. Consider a gate G that consists of two cascaded inverters. Suppose that $t_{pd(G)} > t_{cont}(G) > 0$ and that $t_{su}(FF), t_h(FF) > 0$.

   (a) Show how G together with a FF can be used to build a new Flip-Flop, called FF', for which $t_h(FF') < 0$. Write all the characteristics of FF' in terms of those of FF and G (i.e. setup time, contamination delay, and propagation delay).

(b) Show how G together with a FF can be used to build a new Flip-Flop, called FF'', for which $t_{su}(FF'') < 0$. Write all the characteristics of FF' in terms of those of FF and G (i.e. hold time, contamination delay, and propagation delay).

5. In the definition of synchronous circuits, we required that the clock signal feed only the clock ports of flip-flops. Consider the circuit depicted in Figure 1 that violates this requirement. Proper functioning of the D-FF (and hence the circuit) is guaranteed only if setup and hold time requirements are satisfied. Under which conditions can the signal feeding the D port of the D-FF satisfy the setup and hold time requirements?

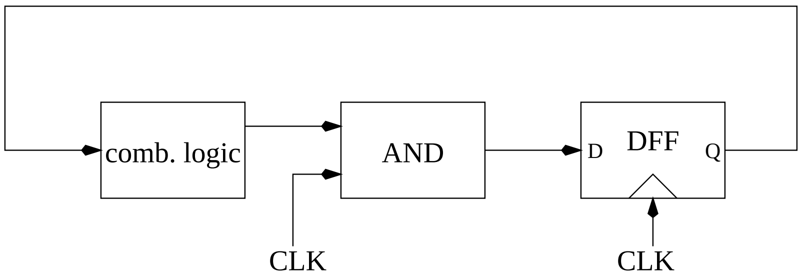

Figure 1: A "synchronous" circuit in which the clock feeds also a gate.

6. In the definition of synchronous circuits, we required that the clock ports of flip-flops be fed only by the clock signal. Consider feeding the clock port of a D-FF by combinational logic. Obviously, glitches (i.e. non monotonous transitions between logic levels for periods of time that are shorter than the propagation delay) can cause errors in such a situation because glitches might cause unwanted "rising edges". Consider the circuit depicted in Figure 2 in which a "glitch-free" combinational circuit feeds the clock port of the D-FF. Proper functioning of the D-FF (and hence the circuit) is guaranteed only if setup and hold time requirements are satisfied. Under which conditions can the signal feeding the D port of the D-FF satisfy the setup and hold time requirements?

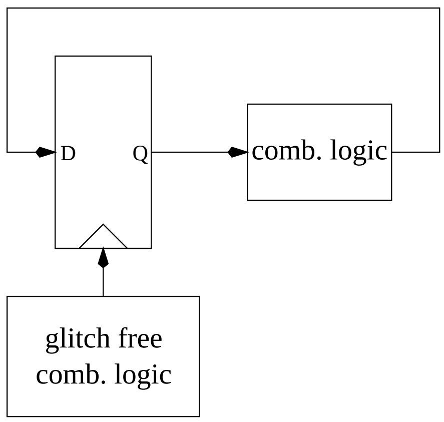

Figure 2: A "synchronous" circuit in which combinational logic feeds the clock port of a D-FF.