Introduction to Digital Computers - Spring 2000

Assignment No. 7

Course homepage: http://www.eng.tau.ac.il/~guy/Digital_Computers00/

Firm Deadline: May 18th

Questions:

1. Organization of the main memory: multiple memory banks. Show how the main memory of the DLX can be built from RAMs that are 8 bits wide. Your organization should be able to support addressing of bytes, half words, and words, provided that the address of a half word is even and the address of a word is divisible by 4. (The case that the remainder mod 4 of the address does not match the width of the accessed string is called *misaligned access*. A misaligned access fails, namely, a write has no effect and a read returns undefined data.) The inputs to the main memory are: Adr[31 : 0], w (signaling whether this is a write operation), D_in[31 : 0], and IR[27 : 26] (00 - means addressing a byte, 01 - means addressing a half word, and 11 - means addressing a word). The output is D_out[31 : 0] and misa (signaling whether the access is misaligned).

2. Specifying the connectivity of the datapath. Consider the following datapath environments: GPR, IR, PC, ALU, Shifter, Memory. For each environment, list the origins of the inputs and destinations of the outputs needed to support DLX instructions in each control state (don't forget the MDR and the MAR).

3. Show that the datapath of the DLX supports the connectivity required in Question 2.

4. Consider the instructions: lb, sb, addi, andi, sgri, beqz, slli, sll, add, and, j, jal. Show the flow of data in the datapath during the execution of these instructions (no need to deal with fetch and decode).