Intro. to Digital Computers - Spring 2000 Plan

chapter	#	date	topic
Hardware	1.	22.02	Tirgul: Xilinx Foundation - schematic entry and simulation
Design Tools	2.	24.02	Tirgul: Xilinx Foundation - VHDL (finite state machine)
Combinational	3.	29.02	Combinational Circuits: definitions, simulation theorem, delay and cost
Circuits	4.	02.03	Vector Notation, Combinational Modules I (half-decoder, decoder, OR-tree, zero tester)
	5.	07.03	Combinational Modules II (encoder), Adder I (ripple-carry adder), Carry Bits, Adder II (divide & conquer, conditional-sum adder)
	6.	09.03	Adder III (parallel prefix adder)
	7.	14.03	Signed Addition (two's complement: definition and properties, main theorem: reduction of signed addition to unsigned addition, implementation), two's complement adder/subtracter.
	8.	16.03	*Multipliers (unsigned & signed)
		21.03	Purim Vacation
Synchronous	9.	23.03	Synchronous Systems: definition, clock, D-latch, edge triggered flip-flop, the arbitration problem
Systems	10.	28.03	Functionality (restricted case: only gates and FF's), Minimum Clock Period & Timing Verification
	11.	30.03	Additional Components (driver, bus, RAM, ROM, clock enabled register), Functionality (with drivers and memories)
	12.	04.04	Synthesis of Finite State Machines I
	13.	06.04	Synthesis of Finite State Machines II
Mid-Term Exam			

chapter	#	date	topic
DLX	14.	11.04	Overview & Instruction Set
	15.	13.04	DLX programming
	16.	02.05	Instructions Execution Flow I
	17.	04.05	Instructions Execution Flow II
		09.05	Yom Hazikaron
	18.	11.05	Control & Datapath: what happens in each state?
	19.	16.05	Implementation of datapath - I
	20.	18.05	Implementation of datapath - II
Precise Interrupt Handling	21.	23.05	Introduction
	22.	25.05	Hardware and Software Support I
	23.	30.05	Hardware and Software Support II
	24.	01.06	Correctness Proof
	25.	06.06	Extensions of The Mechanism

Table 1: Planned schedule (item marked by * will be taught only if time permits)