Introduction to Digital Computers - Spring 1997

Assignment No. 10

Course homepage:

http://www.eng.tau.ac.il/~guy/Digital_Computers/dc_home.html

Deadline: 2 June

1. Consider the computation of the effective address for accessing the memory in the DLX:
$$\text{effective address} = RS1 + Sext(Imm)$$
Discuss the following issues: Is this operation an unsigned addition or a signed addition? What happens if this addition overflows? What happens if this addition results with a negative value? Should these situations cause an interrupt?

2. Suppose that R1 is used as a "channel" between the interrupt stack and the special registers during "restore status" in interrupt handling. How can we restore R1 if we did not save it during "restore status"?

3. Yankel wanted to improve and simplify the communication between the special registers and the interrupt stack. He suggested adding an instruction for loading values from the main memory to the special registers (and also an analogous "store" instruction). Discuss whether this can be implemented on the proposed datapath of the DLX.

4. The functionality of the cause register (CA) is given by
$$CA[i](t{+}1) = \begin{cases} reset \vee pup \vee (CA[0](t) \wedge not(\text{clear\_CA}[t]) & \text{if } i = 0 \\ evn[i](t) & \text{if } i \in [31:7] \\ (evn[i] \wedge SR[i](t)) \vee (CA[i](t) \wedge not(\text{clear\_CA}[t])) & \text{if } i \in [6:1] \end{cases}$$
Design the CA environment.

5. Write a table with a column for every special register and a row for every control state that effects the contents of the special registers. Fill the table with the information describing what happens to the special registers during these control states.