Introduction to Digital Computers - Fall 1997

Assignment No. 2

Course homepage: http://www.eng.tau.ac.il/~guy/Digital_Computers/dc_home.html

Deadline: March 24th

1. Consider the problem of designing a decoder with inputs $x[0 : n \Leftrightarrow 1]$ and outputs $y[0 : 2^n \Leftrightarrow 1]$.

   (a) Design the best combinational decoder you can (emphasize minimization of delay!) Write the (recurrence) equations for the delay and cost of the resulting decoder.

   (b) Compare the cost and delay of the "your" decoder with the cost and delay of the decoder presented in class for values: $2 \leq n \leq 128$. (Refer to both technologies: "Motorola" and "Venus"). It is recommended that you write a program to compute the costs and delays, and even draw the graph comparing the costs and the delays.

   (c) Compute the parameter of equal quality eq for the above values of n.

   (d) If $q \in [0.2, 0.5]$, which design is better for the above values of n?

2. The *fanout* of a net is the number of gate inputs that are fed by the net. In many technologies the fanout is limited. In such cases, a gate-output that needs to be fed to many gate-inputs must pass through a "buffer" (that deals with amplifying and restoring the voltage). A d-buffer is a gate that has 1 input and d outputs, and all the output values equal the input value.

   Suppose that the fanout is limited by 2, and that one may use 2-buffers the cost of which equals 1 and the delay of which equals 1.

   Suppose that a gate-output has to be fed to 2^k gate-inputs. What is the best way to distribute the signal using 2-buffers? Prove that your suggestion is optimal.

3. Suppose that the fanout is limited by 2, and that one may use 2-buffers the cost of which equals 1 and the delay of which equals 1.

   (a) Rewrite the recurrence equations for the delay and cost of the two types of decoders from Question 1.

   (b) Recompute the cost and delays of the two types of decoders for $2 \leq n \leq 128$.

   (c) Recompute the parameter of equal quality eq for the above values of n.

   (d) If $q \in [0.2, 0.5]$, which design is better for the above values of n?

4. Design a tester for zero. The input is n bits $x[0 : n \Leftrightarrow 1]$, and the output $z \in \{0, 1\}$ satisfies:

$$z = 1 \Leftrightarrow (x_0 = 0) \wedge (x_1 = 0) \wedge \cdots \wedge (x_{n-1} = 0)$$

   Write the cost and delay equations of the zero tester.