Introduction to Digital Computers - Spring 1999

Assignment No. 6

Course homepage: http://www.eng.tau.ac.il/∼guy/Digital_Computers99/dc_home.html

Firm Deadline: June 9th - before the beginning of the lecture.

Questions:

1. Design a Mux-Tree(n). Prove the correctness of your design.

   Input: $d[k-1:0], s[\ell-1:0]$, where $k = 2^{\ell}$.

   Output: $z \in \{0,1\}$.

   Specification: $z = d[\langle s[\ell-1:0]\rangle]$.

2. Let S denote a synchronous circuit in which all the flip-flops have the same critical interval, C, and the same interval, A, in which the output may change. Prove: if $A \cap C$ is empty, then there exists a minimum clock period Φ^* such that, for every clock period $\Phi \geq \Phi^*$, the circuit S functions properly.

3. Consider a gate G that consists of two cascaded inverters. Suppose that $t_{pd(G)} > t_{cont}(G) > 0$ and that $t_{su}(FF), t_h(FF) > 0$.

   (a) Show how you can use G in order to make the hold time of a flip-flop negative. How does your change effect the other characteristics (setup time, contamination delay, and propagation delay) of the flip-flop?

   (b) Show how you can use G in order to make the setup time of a flip-flop negative. How does your change effect the other characteristics (hold time, contamination delay, and propagation delay) of the flip-flop?

4. Consider a synchronous circuit with control, S, (consisting of gates, flip-flops, memories, drivers, and nets).

   (a) Write an algorithm for determining the minimum feasible clock cycle Φ^* of S.

   (b) Prove the correctness of your algorithm. You may rely on the algorithm for computing the minimum feasible clock cycle of a synchronous circuit.

   (c) What is the complexity of your algorithm?