Introduction to Digital Computers - Spring 1999

Assignment No. 7

Course homepage: http://www.eng.tau.ac.il/~guy/Digital_Computers99/dc_home.html

Firm Deadline: June 16th - before the beginning of the lecture.

Questions:

1. Organization of the main memory: multiple memory banks. Show how the main memory can be built from RAMs. Assume that access to a RAM reads or writes a byte. Your organization should be able to support addressing of bytes, half words, and words. The inputs to the main memory are: Adr[31 : 0], w (signaling whether this is a write operation), D_in[31 : 0], D_out[31 : 0], and IR[27 : 26] (00 - means addressing a byte, 01 - means addressing a half word, and 11 - means addressing a word). The output is D_out[31 : 0].

2. Specifying the datapath. Consider the following datapath environments: GPR, IR, PC, ALU, Shifter. For each environment, list the origins of the inputs and destinations of the outputs needed to support DLX instructions.

3. Show that the datapath of the DLX supports the connectivity required in Question 2.

4. Consider the instructions: lb, sb, addi, andi, sgri, beqz, slli, sll, add, and, j, jal. Show the flow of data in the datapath during the execution of these instructions (no need to deal with fetch and decode).