Introduction to Digital Computers - Spring 1999

Assignment No. 9

Course homepage: http://www.eng.tau.ac.il/∼guy/Digital_Computers99/dc_home.html

Firm Deadline: June 30th - before the beginning of the lecture.

Questions:

1. Upper bound on the response time of handling interrupts. Two definitions:

   (a) Interrupt i *occurs* in clock cycle t if $evn[i](t) = 1$ and $evn[i](t-1) = 0$.

   (b) Interrupt i is *caught* in clock cycle t if $CA[i](t+1) = 1$ (namely, $CA[i]$ sampled a 1 in the end of cycle t and outputs a 1 in the begining of cycle $t+1$).

   Suppose that interrupt i is caught in cycle t. Give an upper bound on t', the clock cycle in which the control has a transition from JISR2 to "fetch" with $ECA[i](t') = 1$.

   Remark: assume that an access to the memory takes at most WS cycles.