Computer Arithmetic - Spring 1998

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http://www.eng.tau.ac.il/~guy/Computer_Arithmetic/arith_home.html

Assignment Number 3

Deadline: beginning of class on April 23rd

1. (sign-magnitude subtraction) Design a circuit with inputs $a, b \in \{0,1\}^n$ that outputs $s \in \{0,1\}^n$, $sign \in \{0,1\}$ such that
$$(-1)^{sign} \cdot \langle s \rangle = \langle a \rangle - \langle b \rangle$$
Prove the correctness of your design. The delay of your design should be only greater than the delay of an adder by an *additive* constant.

2. Consider the array multiplier depicted below. Describe the functionality of the "circles". Prove the correctness of the design. Extend the design to handle multiplication of numbers encoded in two's complement. Prove the correctness of your extension. Apply the extension to adding partial products in logarithmic time (using 4:2-adders and the divide-and-conquer addition tree).

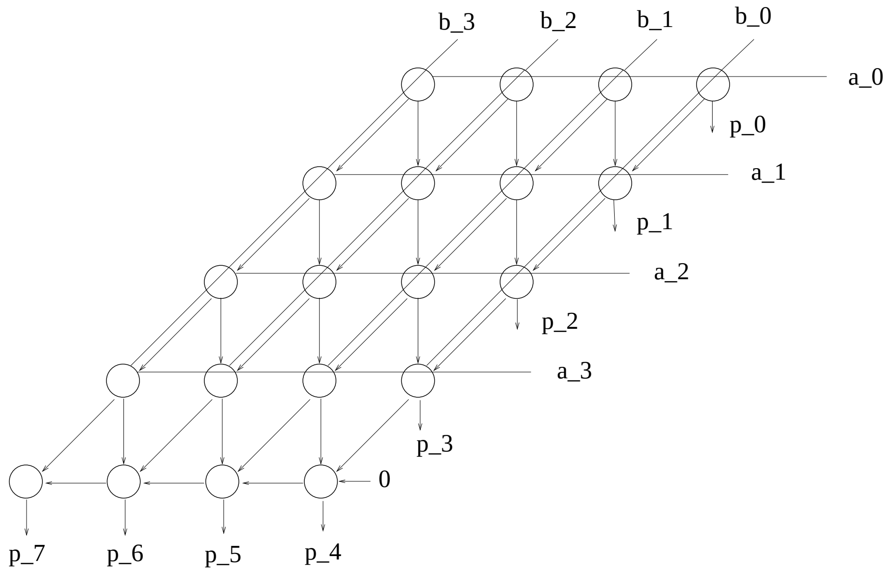

Figure 1: array multiplier - unsigned numbers

3. Compare the cost and delay of an adder tree based on 3:2-adders and an adder tree based on 4:2-adders, when used for multiplying $n \times n$ unsigned numbers. Write the recurrence equations, and compute the values for $n = 16, 23, 32, 52, 64$.