Computer Arithmetic - Spring 1998
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http://www.eng.tau.ac.il/~guy/Computer_Arithmetic/arith_home.html

Assignment Number 6 - Final Exam

Deadline: July 5th, 12:00 (noon) in my mailbox (room 124, Labs Building)

Submission must be printed - not handwritten (except for drawings). Submission must start with a signed declaration stating that you did the work by yourself according to the university rules regarding submissions of assignments (see the university catalog).

1. (40%) Design the fastest circuits you can for the following tasks:

   (a) counting number of leading zeros in binary.
   Input: binary string $a_1 a_2 \cdots a_n \in \{0,1\}^n$ (assume $n = 2^k$).
   Output: binary string $b = b_{k-1} b_{k-1} \cdots b_0$ such that

   $$\begin{aligned} \langle b \rangle > 0 &\Rightarrow \forall i \leq \langle b \rangle \ : \ a_i = 0 \\ \langle b \rangle < n &\Rightarrow a_{\langle b \rangle + 1} = 1 \end{aligned}$$

   (b) counting the number of leading zeros in unary.
   Input: binary string $a_1 a_2 \cdots a_n \in \{0,1\}^n$
   Output: binary string $z = z_1 z_2 \cdots z_n$ such that

   $$z_i = 1 \iff \bigwedge_{j \leq i} a_j = 0$$

   Guidelines:

   i. State very clearly what method your design is based on. Use a “high-language” to explain the method and do not explain your design in terms of “bits”.
   ii. Prove the correctness of your design.
   iii. Analyze the cost and delay of your design (write the recurrence equations and the asymptotics).

2. (60%) Design a multiplier of (unsigned) binary encoded numbers that uses Booth radix 8 recoding (i.e. digit set is $\{-4, \ldots, 4\}$).

   (a) Explain in detail how the recoding is implemented.
   (b) Explain how to pre-process the partial products $\langle A \rangle \cdot b'_i$, where A denotes the multiplicand and b'_i denotes the i'th digit of the recoded multiplier.
   (c) State a claim (and prove it) that formalizes that the preprocessing allows one to use unsigned addition for adding the pre-processed partial products.
   (d) Explain in detail how a “row” in the multiplier (i.e. the circuit that combines A and b'_i) is implemented.
   (e) Analyze the cost and the delay of the multiplier (recurrence equations and asymptotics). Solve the recurrence equations for operands of $n = 32, 53, 64, 128$ bits.
   (f) Show how to extend your design to handle two's complement encoded numbers. Prove the correctness of your modification. Analyze the cost and delay of the modification.