Indium oxide Schottky junctions with InP and GaAs

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Junctions of transparent conducting oxides on III–V semiconductors have been prepared by deposition of indium oxide layers onto \( p \)-type InP and \( n \)-type GaAs by means of reactive evaporation of In in the presence of oxygen at different substrate temperatures. The electrical properties and chemical composition of these junctions have been investigated using current-voltage measurements in the dark at room temperature, capacitance-voltage measurements, and depth profiling by Auger electron spectroscopy. The best diodes were obtained by deposition at a substrate temperature near 250 °C and oxygen pressure of \( 5 \times 10^{-4} \) Torr. These diodes exhibit a Schottky barrier height of 0.80 eV for \( n \)-type GaAs and 0.87 eV for \( p \)-type InP with an ideality factor of 1.04. The Schottky barrier height decreases with decreasing deposition temperature for both substrates. The roles of the tunneling-transparent interface layer and interface region are theoretically considered. It is shown that as the deposition temperature is increased, the barrier height increases due to the accompanying reduction in the density of surface states, which are induced by elemental In at the interface.

I. INTRODUCTION

Interest in transparent conducting oxides (TCO) as top contacts in optoelectronic applications has been increasing recently. The high transparency of these layers up to infrared radiation, together with their high reflectivity in the infrared and high free carrier concentration make them very attractive for optoelectronic device fabrication.\(^1\)\(^{-12}\) TCO films are expected to play a key role in existing and novel structures, based on the fast growing technology of the III–V group. One example is obtaining a radiation resistant solar cell, which is an important goal of the ongoing research on space power systems. Recently, it has been reported that InP solar cells have greater radiation resistance than Si and even GaAs cells.\(^5,7\)

In view of the success of solar cells based on indium tin oxide (ITO) contacts sputtered on \( p \)-type InP\(^3,4,7,8\) and evaporation of pure In (or In:Sn alloy 90:10) under oxygen pressure on \( n \)-type GaAs\(^9\)–\(^12\) we have focused our study on the preparation and investigation of Schottky diodes based on indium oxide/\( p \)-type InP structures. The diodes were fabricated by reactive evaporation of pure In under oxygen pressure. Using this method eliminates sputtering damage of the semiconductor substrate surface. In order to investigate the properties of the indium oxide, a comparison of the characteristics of diodes based on indium oxide/\( p \)-type InP and indium oxide/\( n \)-type GaAs structures, fabricated using the same deposition parameters, was carried out.

II. EXPERIMENTAL

The samples used were (100) oriented \( n \)-type GaAs wafers (Si doped to \( 5 \times 10^{16} \) cm\(^{-3} \)) and (100) oriented \( p \)-type InP wafers (Zn doped to \( 5 \times 10^{16} \) cm\(^{-3} \)). Back contacts were formed by deposition of layers of Au (1000 Å) on Ge (100 Å) on the \( n \)-type GaAs substrates, followed by vacuum annealing for 30 min at 420 °C and by depositing layers of Au (200 Å), Zn (400 Å), Au (2000 Å) on the \( p \)-type InP substrates followed by vacuum annealing for 10 min at 400 °C. The top surface was mechanically polished and etched in 0.3% BrMe solution for about 1 min, just before being loaded into the deposition chamber (base pressure \( 1 \times 10^{-6} \) Torr). The semiconductor substrates were heated up to 350 °C during 10 min. After this degassing process, the substrate temperature was decreased to the deposition temperature \( (T_{\text{dep}}) \). The different deposition temperatures were carried out at substrate temperatures from 100 °C up to 250 °C. Indium (99.99%) was resistively evaporated onto the InP or GaAs substrates under a pressure of \( 5 \times 10^{-4} \) Torr of \( O_2 \), which reacted with the deposited In at the substrate surface. Control of the rate of evaporation and the thickness was done by means of a quartz crystal oscillator during deposition. The final film thickness was about 1000 Å and the deposition rate was 1 Å/s. The diodes were fabricated through a stainless steel mask with different holes with areas of 0.08, 0.008, and 0.003 cm\(^2\).

Current-voltage (\( J-V \)) characteristics in the dark were measured with a bias resolution of 3 mV and an average noise signal of 15 pA. Diodes of practically identical current densities have been obtained for each of the given three different sizes.

Auger electron spectroscopy (AES) with simultaneous depth profiling was carried out using a 3 keV, 0.5 \( \mu \)A electron beam with a spot size of 5 μm electron beam and a double-pass cylindrical mirror analyzer. Depth profiling was obtained by a 1 keV, 10 \( \mu \)A Ar\(^+\) ion beam. The AES signal was calibrated for lineshape and atomic concentration using standard spectra of an In\(_2\)O\(_3\) (99.997% pure) sample, as well as cleaved GaAs and InP samples. The spectra were taken at intervals corresponding to removal of about 30-Å-thick layers.

III. RESULTS

A set of three indium oxide/\( p \)-type InP and three indium oxide/\( n \)-type GaAs diodes, obtained under different
deposition temperatures, was chosen for the forward $I-V$ and $C-V$ measurements. The $I-V$ characteristics of the indium oxide/p-type InP diodes are shown in Fig. 1 and compared with the best indium oxide/n-type GaAs diode. The forward $I-V$ characteristics of the diodes can be well fitted by the Schottky formula with the parameters displayed in Fig. 1. The ideality factor ($\eta$) of all diodes is very close to unity ($\eta=1.03-1.04$) and, therefore, the thermionic emission mechanism may be assumed. We note that $\eta$ of both indium oxide/p-type InP and indium oxide/n-type GaAs diodes is not sensitive to changes in $T_{\text{dep}}$. This is in contrast with the dependence, reported recently in Refs. 9 and 10, for indium oxide/n-type GaAs diodes obtained by the same method under various preparation conditions. The main process difference lies in the additional degassing process, preceding the indium deposition in our case. It seems that such a degassing step provides cleaner substrate surfaces with a relatively low density of electronic states at the resulting interface and thus low $\eta$ values.

The barrier height ($\phi$), determined by the forward $I-V$ characteristics, varies in the range $\phi=0.84-0.87$ eV for indium oxide/p-type InP and $\phi=0.76-0.80$ eV for indium oxide/n-type GaAs diodes. The upper limit of this range corresponds to the highest $T_{\text{dep}}$. This fact is in good agreement with the optimal deposition parameters reported in Refs. 9-12. The barrier height decreases for both types of diodes with decreasing $T_{\text{dep}}$.

A plot of $C^{-2}$ as a function of $V$ yields a straight line, the intercept of which with the $V$ axis determines $\phi$. Results of $C-V$ measurements lead to slightly higher values than those obtained by $I-V$ measurements, namely $\phi=1.1$ and 1.02 eV for indium oxide/p-InP and indium oxide/n-type GaAs diodes, respectively, at $T_{\text{dep}}=250^\circ$C.

The diodes were also investigated using AES depth profiling. The obtained profiles are of the type shown in Fig. 2 (top frame) for $T_{\text{dep}}=100^\circ$C. The ratio of In to O concentrations is constant in the oxide bulk for all tested diodes. The atomic concentration of O is about 60%, which corresponds to stoichiometric In$_2$O$_3$ layers. The layer stoichiometry is independent of $T_{\text{dep}}$, in accordance with previously obtained results on GaAs.$^{9,10}$ The situation is quite different in the interface region. The measured width of the interface region, varies with $T_{\text{dep}}$ and increases, up to 20% of its value, at $T_{\text{dep}}=100^\circ$C, with increasing $T_{\text{dep}}$ in the tested range. This trend may be explained either by a possible measurement error due to sputtering-induced roughness of the diode surface, or by enhanced interdiffusion of O and P (or As), which takes place at the interface (Fig. 2). This process leads to perturbation of the crystal stoichiometry in the interface region and to defect formation.

The shape of the In MNN Auger line in the InP substrate (elemental In) comprises two peaks with energy positions at 402 eV ($\text{In}_1$) and 408 eV ($\text{In}_2$) (see the spectrum taken at curve $t=26'$ in Fig. 2, bottom frame). The ratio of the peak intensities is $I_{\text{In}_1}/I_{\text{In}_2}\approx1.1$. The same In line of oxidized indium has two peaks, which are shifted to $I_{\text{In}_1}=399$ eV and $I_{\text{In}_2}=405$ eV, and their intensity ratio is $I_{\text{In}_1}/I_{\text{In}_2}\approx0.9$ (see the spectrum taken at $t=12'$ in Fig. 2, bottom frame). It is noted that the absolute value of the shift depends on the analyzer resolution. These changes in the In MNN line correspond to differences in the In chemical bonding.$^{13-15}$ The shape of the In line is quite different.
at the indium oxide/p-type InP interface (see the spectrum taken at \( t=22' \) in Fig. 2, bottom frame). In this case, the In line comprises three peaks. This lineshape seems to be a superposition of the lines of elemental and oxidized In, i.e., the In is observed in the both possible chemical states.

Analyses of the In\(_1\)/In\(_2\) ratio, described in Refs. 13–15 and Ref. 10, show the presence of unoxidized elemental In at the interface in both GaAs and InP based diodes at low \( T_{\text{dep}} \) (100 °C).

## IV. DISCUSSION

Our results show that increasing \( T_{\text{dep}} \) leads to the following important changes in the interface structure and composition: The concentration of elemental In at the interface is reduced; The width of the interface region and the apparent associated nonstoichiometry increase. It also leads to changes in the electrical characteristics, i.e., the Schottky barriers of both n- and p-type diodes increase. Let us examine the possible correlation of these two types of changes.

Elemental In can form metallic clusters at the interface and/or it can induce local interface states.\(^{16,17}\) In both cases, the measured barrier height may be different from the ideal oxide–semiconductor interface. This could be a consequence of the parasitic diode, based on the metallic clusters/semiconductor junction, or of the band bending induced by the interface states, respectively.

Let us consider these two cases.

### A. The parasitic diode effect

In the case of metallic cluster formation of In at the interface, the investigated junction (denoted by index 0) can be considered as comprising two diodes with different areas (\( S_1 \) and \( S_2 \)) and barrier heights (\( \phi_0 \) and \( \phi_2 \)) in parallel. Diode 1 is the true indium oxide/p-type InP (or indium oxide/n-type GaAs) junction. Diode 2 is the parasitic In/p-type InP (or In/n-type GaAs) junction. Obviously, the measured current is the sum of the currents through diodes 1 and 2:

\[
I_0 = I_1 + I_2 ,
\]

(1)

where each of these currents can be represented by the Schottky formula:

\[
I_i = A^{**}S_i/t^2 \exp \left( -\frac{q\phi_i}{kT} \right) \left[ \exp \left( -\frac{qV}{\eta_i kT} \right) - 1 \right] ,
\]

(2)

where \( A^{**} \) is the Richardson constant and \( \eta_i \) is the ideality factor of diode \( i \).

In order to simplify the following analysis, the ideality factor of each diode is taken as unity (see Fig. 1). The measured barrier height (\( \phi_0 \)) can be represented by the following expression:

\[
\phi_0 = \phi_1 + \Delta \phi ,
\]

(3)

where \( \Delta \phi \) is the difference between the measured and true barrier heights, which is due to the presence of the parasitic diode. \( \Delta \phi \) can be obtained from Eqs. (1)–(3) (in the relevant case where \( V > 3kT/q \)):

\[
\Delta \phi = -\frac{kT}{q} \ln \left[ 1 + \frac{S_2}{S_0} \left( \exp \left( -\frac{q(\phi_2 - \phi_1)}{kT} \right) - 1 \right) \right] .
\]

(4)

Thus, \( \Delta \phi \) is a function of the ratio \( S_2/S_0 \) and of the relative barrier height (\( \phi_2 - \phi_1 \)). Figure 3 shows \( \Delta \phi \) as a function of \( S_2/S_0 \) with \( \phi_2 - \phi_1 \) as a parameter. Our experimental results show that \( \phi_0 \) (and consequently \( \Delta \phi \)) increases with \( T_{\text{dep}} \), accompanied by a reduction of \( S_2/S_0 \) (due to the decreasing concentration of In clusters). Figure 3 shows that this occurs only for negative values of \( \phi_2 - \phi_1 \). However, in our case, the relative barrier height is positive, according to reported experimental data\(^{19}\) (e.g., for InP \( \phi_2 = 0.89 \) eV, which is higher than \( \phi_1 = 0.87 \) eV). Therefore, the parasitic diode effect on the barrier height is apparently negligible.

### B. The effect of the interface parameters

We consider the interface as comprising two regions: a tunneling–transparent interface layer\(^{18}\) and the interface region. The tunneling–transparent interface layer can be characterized by the following parameters: its thickness (\( \delta \)), permittivity (\( \epsilon_i \)), and density of surface states (\( D_s \)). In the present study, we assume that the tunneling–transparent interface layer parameters are independent of the diode type due to the relatively low doping concentrations in our samples (less then \( 5 \times 10^{16} \text{ cm}^{-3} \)). The interface region is a result of interdiffusion, creating a defective layer at the interface. Such defects may affect the free carrier concentration and lifetime in the interface region relative to the bulk values. Therefore, in the following discussion the interface region will be characterized by the following parameters: its width (\( W_{\text{int}} \)), free carrier concentration (\( n \) or \( p \)), and their lifetimes (\( \tau \)). \( W_{\text{int}} \) depends mainly on the interdiffusion coefficients and can reach tens and even hundreds of angstroms. The free carrier concent...
tration can vary in a wide range, depending on the defect type. The latter may cause a partial compensation relative to the bulk doping, and even a conversion of the conductivity type in the interface region. Thus, the nature of the interface region is extremely different from that of the tunneling-transparent interface layer.

In our case, which deals with relatively low doping concentrations, $\phi$ can be represented by the well-known approximation, $^{18}$ for $n$-type Schottky diodes:

$$\phi^n = c_2 (\phi_m - \chi) + (1 - c_2) \left( \frac{E_g}{q} - \Phi^n \right),$$

and for $p$-type Schottky diodes:

$$\phi^p = c_2 \left( \frac{E_g}{q} + \chi - \phi_m \right) + (1 - c_2) \Phi^p.$$  

Here $E_g$ and $\chi$ are the semiconductor band gap and its affinity; $\phi_m$ is the indium oxide work function; $\Phi^{n(p)}$ is the free surface Fermi level position relative to the valence band edge of the of $n$- ($p$-) type semiconductor:

$$\Phi^n = \frac{E_g}{2q} \ln \left( \frac{n}{n_i} \right),$$  

$$\Phi^p = \frac{E_g}{2q} \ln \left( \frac{p}{n_i} \right),$$

where $n_i$ is the intrinsic carrier concentration (Boltzmann statistics is assumed).

The tunneling-transparent interface layer effect on the barrier height can be expressed by an integral parameter ($c_2$):

$$c_2 = \frac{e_i}{e_i + q^2 \delta D_i}.$$  

(7)

When $c_2$ is close to 0, $\phi$ is strongly affected by the tunneling-transparent interface layer; when $c_2$ is close to 1, the effect of the tunneling-transparent interface layer is negligible.

In order to examine the dependence of $\phi$ on $T_{\text{dep}}$, we assume that only $n$ ($p$) and $c_2$ are sensitive to $T_{\text{dep}}$. Let us consider two limiting cases: The variation rate of $n$ ($or$ $p$) with $T_{\text{dep}}$ is much higher than that of $c_2$ (the interface region, and not the tunneling-transparent interface layer, plays the dominant role), and vice versa.

1. The effect of the interface region on the barrier height

In this first limiting case, $c_2$ can be assumed as independent on $T_{\text{dep}}$. Figures 4(a) and 4(b) show $\phi$ as a function of the free carrier concentrations ($n$ and $p$) with $c_2$ as a parameter for GaAs and InP, respectively. The graphs show that decreasing the free carrier concentration in the interface region (toward $n_j$) results in increasing $\phi$. Such a decrease can be caused by partial compensation in the interface region due to an increase of the defect concentration and their diffusion lengths with increasing $T_{\text{dep}}$. Consequently, the observed increase of $\phi$ with $T_{\text{dep}}$ could possibly be a result of doping compensation in the interface region.

2. The effect of the tunneling-transparent interface layer on the barrier height

In the second limiting case, $n(p)$ is assumed to be independent on $T_{\text{dep}}$. Figures 5(a) and 5(b) show $\phi$ as a function of $c_2$ with $\Phi$ as a parameter for GaAs and InP, respectively. Unfortunately, there are no reliable experimental data in the literature for the dependence of $c_2$ on $T_{\text{dep}}$. Therefore, two possible trends should be considered.

(1) The effect of the tunneling-transparent interface layer on $\phi$ increases, i.e., $c_2$ decreases from 1 to 0 with $T_{\text{dep}}$ [see Eq. (7)]. Figure 5 shows that this trend leads to increasing $\phi$ (as observed experimentally) for $\Phi^p=0.9$ and $1$.

Figure 4 shows that in order to yield the observed high values of $\phi$, $c_2$ must be close to unity. Also, according to Fig. 4, the measured increase of $\phi$ with $T_{\text{dep}}$ (approximately 0.04 eV) may be achieved, only by high compensation in the interface region ($n_j$). However, the measured ideality factors, which are close to unity, indicate a low defect density. Thus, it is not physically plausible that the necessary high compensation is accompanied by the unchanged values of $\eta$. Therefore, there does not seem to be any significant effect of the interface region on $\phi$. The reason that a finite $T_{\text{dep}}$-dependent $W_{\text{int}}$ is observed by AES depth profiling has to be due to enhanced surface roughness of the indium oxide film with $T_{\text{dep}}$.
eV, and for $\Phi^d=0.1$ and $0.3$ eV for both substrates. According to the values of $\Phi^d$ of these lines, they represent cases where $E_F$ is close to the valence (conduction) band for n- (p-) type substrates, i.e., $\Phi^d$ is greater than $\Phi^a$. This can occur when the surface states induced by elemental In have a different nature on n- and p-type surfaces. However, this contradicts the assumption that the tunneling-transparent interface layer properties are independent on the substrate type, if it has relatively low doping.\(^1\) Thus, the next trend has to be examined.

(2) The effect of the tunneling-transparent interface layer on $\phi$ decreases i.e., $c_2$ increases from 0 to 1 with $T_{\text{dep}}$ [see Eq. (7)]. Figure 5 shows that this trend leads to increasing $\phi$ for $\Phi^d=0.1$ eV and $0.3$ eV and for $\Phi^d=0.9$ and 1 eV for both substrates. According to the values of $\Phi$ of these lines, they represent cases where $E_F$ is close to the conduction (valence) band for n- (p-) type substrates. This is the usual situation at the free surface of a III-V semiconductor with a low density of states. Moreover, the increase of $c_2$ from 0 to 1 may be provided by a reduction of the elemental In concentration at the interface with increasing $T_{\text{dep}}$ [see Eq. (7)].

In order to examine this last issue, $c_2$ and $\phi_m$ have been calculated using Eqs. (5), (5'), (6), and (6'), for two different deposition temperatures: 100°C and 250°C. In the calculation we have used the measured $\Phi^a$ and $\Phi^d$ and typical values of the material parameters of InP and GaAs: $E_g=1.35$ and 1.42 eV; $\chi=4.40$ and 4.07 eV; $n=p=5\times10^{16}$ cm$^{-3}$, respectively. The work function of indium oxide, determined in this way, $\phi_m=4.88$ eV, and it is independent on either $T_{\text{dep}}$ or the doping type. An identical value is obtained for indium oxide at both InP and GaAs interfaces. Therefore, it can be suggested that the nature of the indium oxide, grown using the present deposition method, is independent on the III-V semiconductor and its properties. However, $c_2$ is found to vary with $T_{\text{dep}}$ from 0.94 to 0.99, in the temperature range from 100°C to 250°C. According to such $c_2$ variation, $D$, must decrease from $7\times10^{11}$ cm$^{-2}$ eV$^{-1}$ at 100°C to $7.7\times10^{10}$ cm$^{-2}$ eV$^{-1}$ at 250°C.

Thus, the increase of the barrier height with increasing $T_{\text{dep}}$ seems to be a direct consequence of the reduction of the density of elemental-In-induced surface states.

V. CONCLUSIONS

Diodes based on indium oxide/p-type InP and on indium oxide/n-type GaAs structures have been fabricated by reactive evaporation of In. The maximum Schottky barrier height of the obtained diodes, is 0.87 eV for indium oxide/p-type, which is greater than the best results obtained for indium oxide/n-type GaAs diodes. Degassing of the semiconductor substrate, prior to the deposition process, leads to improvement of the diode ideality factors ($\eta=1.03/1.04$) at all deposition temperatures ($T_{\text{dep}}=100°C-250°C$).

At the indium oxide/p-type InP interface, the In MNN Auger lineshape is quite different from the one in the bulk of the indium oxide and InP. It suggests that this lineshape is a superposition of the elemental and oxidized In lines, i.e., In is observed in both chemical states.

A comprehensive theoretical analysis of the observed barrier height increase with $T_{\text{dep}}$ is presented. It is shown that such a $\phi$ dependence on $T_{\text{dep}}$ can be explained by a reduction in the density of elemental-In-induced surface states with $T_{\text{dep}}$.

The work function of the indium oxide ($\phi_m=4.88$ eV) is found to be independent on either $T_{\text{dep}}$ or the doping type, at both InP and GaAs interfaces. Therefore, it can be suggested that the nature of the indium oxide, grown using the present deposition method, is independent on the III-V semiconductor and its properties.

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