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Publications

Book

1. S. Weiss and J. E. Smith, *POWER and PowerPC: Principles, Architecture, Implementation*, Morgan Kaufmann Publishers, San Francisco, Calif. 1994. Translated into French and Japanese.

Articles Published In Books

2. S. Weiss and J. E. Smith, "Instruction Issue Logic in Pipelined Supercomputers", *IEEE Transactions on Computers*, Vol. C-33, No. 11, pp. 1013 – 1022, November 1984. Selected to be included in Dharma P. Agrawal (editor), *Advanced Computer Architecture*, IEEE Computer Society Press, 1986.
3. R. Ganesan and S. Weiss, "Scalar Memory References in Pipelined Multiprocessors: A Performance Study", *IEEE Transactions on Software Engineering*, Vol. 18, No. 1, pp. 78–86, January 1992. Selected to be included in C.M. Krishna (editor), *Performance Modeling for Computer Architects*, pp. 302 – 310, IEEE Computer Society Press, 1995.

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4. R. H. Katz and S. Weiss, "A Standard Design Frame for VLSI Circuit Prototyping", *Journal of VLSI and Computer Systems*, Vol. 1, No. 1, pp. 101 – 114, March 1983.
5. S. Weiss and J. E. Smith, "Instruction Issue Logic in Pipelined Supercomputers", *IEEE Transactions on Computers*, Vol. C-33, No. 11, pp. 1013 – 1022, November 1984.
6. J. E. Smith, S. Weiss, and N. Y. Pang, "A Simulation Study of Decoupled Architecture Computers", *IEEE Transactions on Computers*, Vol. C-35, No. 8, pp. 692 – 702, August 1986.
7. S. Weiss, "Scalar Supercomputer Architecture", *Proceedings of the IEEE*, Vol. 77, No. 12, pp. 1970 – 1982, December 1989.
8. S. Weiss and J. E. Smith, "A Study of Scalar Compilation Techniques for Pipelined Supercomputers", *ACM Transactions on Mathematical Software*, Vol. 16, No. 3, pp. 223 – 245, September 1990.
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10. S. Weiss, "Memory Conflict Resolution in Vector Multiprocessors", *Journal of Supercomputing* (Springer Netherlands), Vol. 6, No. 1, pp. 71–85, March 1992.
11. S. Weiss, "Optimizing a Superscalar Machine to Run Vector Code", *IEEE Parallel and Distributed Technology*, Vol. 1, No. 2, pp. 73 – 83, May 1993.
12. S. Weiss and S. Ghahramani, "A Performance Study of Buffered Pseudorandomly Interleaved Memories With Multiple Sections", *Mathematical and Computer Modeling* (Elsevier), Vol. 17, No. 9, pp. 81-87, 1993.
13. S. Weiss, "Increasing the Memory Bandwidth in Superscalar Computers", *Journal of Computer & Software Engineering*, Vol 1, No. 3, pp. 281–297, 1993.
14. J. E. Smith and S. Weiss, "PowerPC 601 and Alpha 21064: A Tale of Two RISCs", *IEEE Computer*, Vol 27, No. 6, pp. 46–58, June 1994.

15. S. Reches and S. Weiss, "Implementation and Analysis of Path History in Dynamic Branch Prediction Schemes", *IEEE Transactions on Computers*, Vol 47, No. 8, pp. 907–912, August 1998.
16. S. Weiss and A. Goldstein, "Floating Point Micropipeline Performance", *Journal of Systems Architecture* (Elsevier), Vol 45, No. 1, pp. 15 –29, Oct. 1998.
17. S. Weiss and E. Finkelstein, "Extending PCI Performance Beyond the Desktop", *IEEE Computer*, Vol 32, No. 6, pp. 80 – 87, June 1999.
18. E. Finkelstein and S. Weiss, "Microprocessor Systems Buses: A Case Study", *Journal of Systems Architecture* (Elsevier), Vol 45, No. 12–13, pp. 1151 – 1168, June 1999.
19. E. Finkelstein and S. Weiss, "Implementation of PCI-based systems using programmable logic", *IEE Proceedings-Circuits, Devices, and Systems* (IEE United Kingdom), Vol 147, No. 3, pp. 171 – 174, June 2000.
20. R. Feig and S. Weiss, "Functional Verification of Instruction Processing Units through Control Flow Modeling," *Microelectronics Journal* (Elsevier), Vol 33, No. 3, pp. 285 – 299, March 2002.
21. E. Finkelstein and S. Weiss, "A PCI Bus Simulation Framework and Some Simulation Results on the PCI Standard 2.1 Latency Limitations," *Journal of Systems Architecture* (Elsevier), Vol 47, No. 9, pp. 807 – 819, March 2002.
22. T. Oved and S. Weiss, "Embedded Instruction Memory in Automotive Engine Controllers," *IEEE Transactions on Vehicular Technology*, Vol 52, No. 1, pp. 173 – 183, Jan. 2003.
23. S. Weiss and R. Tsikel, "Approximate Prefix Coding for System-on-a-Chip Programs," *Journal of Systems Architecture* (Elsevier), Vol 48, No. 13 – 15, pp. 367 – 375, May 2003.
24. S. Weiss and S. Beren, "Class-Based Decompressor Design for Compressed Instruction Memory in Embedded Processors," *IEEE Transactions on Computers*, Vol 52, No. 11, pp. 1495 – 1500, November 2003.
25. T. Karin and S. Weiss, "Programming Windows NT Device Drivers to Operate Non-Interrupting Embedded Devices," *Microprocessors and Microsystems* (Elsevier), Vol 28, No. 1, pp. 27 – 35, February 2004.
26. Y. Sadeh Weinraub and S. Weiss, "Power-Aware Out-of-Order Issue Logic in High-Performance Microprocessors," *Microprocessors and Microsystems* (Elsevier), Vol 30, No. 7, pp. 457 – 467, 2006.
27. R. Gabor, S. Weiss, and A. Mendelson, "Fairness Enforcement in Switch on Event Multithreading," *ACM Transactions on Architecture and Code Optimization*, Vol 4, No. 3, pp. 15, Sept. 2007.
28. A. Golander and S. Weiss, "Hiding the Misprediction Penalty of a Resource-Efficient High-Performance Processor," *ACM Transactions on Architecture and Code Optimization*, Vol 4, No. 4, pp. 6, Jan. 2008.
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31. A. Golander and S. Weiss, "Reexecution and Selective Reuse in Checkpoint Processors," accepted for publication in the *Transactions on High-Performance Embedded Architectures and Compilers* (Springer), scheduled to appear in 2008.

32. A. Golander and S. Weiss, "Checkpoint Allocation and Release," submitted to the *ACM Transactions on Architecture and Code Optimization*, in review.
33. R. Kahn and S. Weiss, "Reducing Leakage Power with BTB Access Prediction," submitted to *Integration, the VLSI Journal* (Elsevier), in review.

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34. R. H. Katz and S. Weiss, "Chip Assemblers: Concepts and Capabilities", *Proceedings 20th ACM/IEEE Design Automation Conferences (DAC '83)*, Miami, Florida, pp. 25 – 30, June 1983.
35. S. Weiss and J. E. Smith, "Instruction Issue Logic for Pipelined Supercomputers", *Proceedings 11th ACM/IEEE Annual International Symposium on Computer Architecture (ISCA '84)*, Ann Arbor, Michigan, pp. 110 – 118, June 1984. The full version of this paper appears as item 5 above in journal papers.
36. S. Weiss, K. Rotzell, T. Rhyne, and A. Goldfein, "DOSS: A Storage System for Design Data", *Proceedings 23rd ACM/IEEE Design Automation Conference (DAC '86)*, Las Vegas, Nevada, pp. 41 – 47, June 1986.
37. S. Weiss and J. E. Smith, "A Study of Scalar Compilation Techniques for Pipelined Supercomputers", *Proc. 2nd ACM/IEEE Int'l Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS II)*, Palo Alto, Cal., pp. 105 – 109, Oct. 1987. The full version of this paper appears as item 8 above in journal papers.
38. S. Weiss, "An Aperiodic Storage Scheme to Reduce Memory Conflicts in Vector Processors", *Proceedings 16th ACM/IEEE Annual International Symposium on Computer Architecture (ISCA '89)*, Jerusalem, Israel, pp. 380 – 385, May 1989.
39. S. Weiss, "Multiple-Port Memory Access in Decoupled Architecture Processors", *Proceedings 20th International Conference on Parallel Processing*, Chicago, Illinois, pp. I-373 – I-376, August 1991.
40. S. Weiss, "Implementing Register Interlocks in Parallel Pipeline, Multiple Instruction Queue, Superscalar Processors", *First IEEE International Symposium on High-Performance Computer Architecture (HPCA '95)*, Raleigh, North Carolina, pp. 14 – 21, Jan. 1995.
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42. E. Federovsky, M. Feder, and S. Weiss, "Branch Prediction Based on Universal Data Compression Algorithms", *Proceedings 25th ACM/IEEE Annual International Symposium on Computer Architecture (ISCA '88)*, Barcelona, Spain, June 1998.
43. S. Weiss and S. Beren, "HW/SW Partitioning of an Embedded Instruction Memory Decompressor", *Proceedings 9th ACM/IEEE Int'l Hardware/Software Codesign Symposium (CODES '01)*, Copenhagen, Denmark, pp. 36 – 41, April 2001. The full version of this paper appears as item 24 above in journal papers.
44. A. Orpaz and S. Weiss, "A Study of CodePack: Optimizing Embedded Code Space," *Proceedings 10th ACM/IEEE Int'l Hardware/Software Codesign Symposium (CODES '02)*, Estes Park, Colorado, pp. 103 – 108, May 2002.
45. R. Gabor, S. Weiss, and A. Mendelson, "Fairness and Throughput in Switch on Event Multithreading," *Proceedings 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO '06)*, Orlando, USA, pp. 149–160, Dec. 2006. The full version of this paper appears as item 27 above in journal papers.

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48. A. Goldstein and S. Weiss, "ePASS – A Software Based POWER Simulator", *7th IEEE Israeli Conference on Computer Systems and Software Engineering*, Herzliya, Israel, pp. 46-54, June 1996.
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50. D. Zeevi and S. Weiss, "Performance of DSP Applications Using Intel's Multimedia Instruction Set Extensions", *Proceedings 1998 IEEE International Conference and Workshop on Engineering of Computer Based Systems*, Jerusalem, Israel, pp. 174 – 178, March 1998.
51. E. Finkelstein and S. Weiss, "PCI Interface Implementation Using CPLD and FPGA Devices," *Proceedings 9th Mediterranean Electrotechnical Conference (Melecon '98)*, Tel-Aviv, Israel, pp. 1284 – 1287, May 1998. The full version of this paper appears as item 19 above in journal papers.
52. T. Karin and S. Weiss, "Programming Windows NT Device Drivers to Operate Non-Interrupting Embedded Devices," *Proceedings 22nd Convention of Electrical and Electronics Engineers in Israel (IEEE)*, Jerusalem, Israel, pp. 105 – 107, Dec. 2002. The full version of this paper appears as item 25 above in journal papers.
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55. S. Grinberg and S. Weiss, "Investigation of Transactional Memory Using FPGAs," *2nd Workshop on Architecture Research using FPGA Platforms (WARFP '06), held in conjunction with the 12th International Symposium on High-Performance Computer Architecture (HPCA)*, Austin, Texas, Feb. 2006.

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1. S. Dasgupta, *Computer Architecture: A Modern Synthesis, Volume 1: Foundations*, Wiley, 1989. (Cites item 5.)
2. M. Johnson, *Superscalar Microprocessor Design*, Prentice–Hall, 1991. (Cites items 5 and 37.)
3. R. J. Baron and L. Higbie, *Computer Architecture*, Addison–Wesley, 1994. (Cites item 5.)
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7. W. Stallings, *Computer Organization and Architecture*, Prentice–Hall, 5th edition, 2000. (Cites items 1 and 5.)
8. S. M. Mueller and W. J. Paul, *Computer Architecture: Complexity and Correctness*, Springer–Verlag, 2000. (Cites item 1.)
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