Shlomo Weiss

13 December 2014

Publications

Articles Published In Books

1. S. Weiss and J. E. Smith, "Instruction Issue Logic in Pipelined Supercomputers," *IEEE Transactions on Computers*, Vol. C-33, No. 11, pp. 1013−1022, November 1984. Selected to be included in Dharma P. Agrawal (editor), *Advanced Computer Architecture*, IEEE Computer Society Press, 1986.

2. R. Ganesan and S. Weiss, "Scalar Memory References in Pipelined Multiprocessors: A Performance Study," *IEEE Transactions on Software Engineering*, Vol. 18, No. 1, pp. 78−86, January 1992. Selected to be included in C.M. Krishna (editor), *Performance Modeling for Computer Architects*, pp. 302−310, IEEE Computer Society Press, 1995.

Book

1. S. Weiss and J. E. Smith, *POWER and PowerPC: Principles, Architecture, Implementation*, Morgan Kaufmann Publishers, San Francisco, Calif. 1994. Translated into French and Japanese.

Refereed Articles in Journals

2. R. H. Katz and S. Weiss, "A Standard Design Frame for VLSI Circuit Prototyping," *Journal of VLSI and Computer Systems*, Vol. 1, No. 1, pp. 101−114, March 1983.

3. S. Weiss and J. E. Smith, "Instruction Issue Logic in Pipelined Supercomputers," *IEEE Transactions on Computers*, Vol. C-33, No. 11, pp. 1013−1022, November 1984.

4. J. E. Smith, S. Weiss, and N. Y. Pang, "A Simulation Study of Decoupled Architecture Computers," *IEEE Transactions on Computers*, Vol. C-35, No. 8, pp. 692−702, August 1986.

5. S. Weiss, "Scalar Supercomputer Architecture," *Proceedings of the IEEE*, Vol. 77, No. 12, pp. 1970−1982, December 1989.

6. S. Weiss and J. E. Smith, "A Study of Scalar Compilation Techniques for Pipelined Supercomputers," *ACM Transactions on Mathematical Software*, Vol. 16, No. 3, pp. 223−245, September 1990.

7. R. Ganesan and S. Weiss, "Scalar Memory References in Pipelined Multiprocessors: A Performance Study," *IEEE Transactions on Software Engineering*, Vol. 18, No. 1, pp. 78−86, January 1992.

8. S. Weiss, "Memory Conflict Resolution in Vector Multiprocessors," *Journal of Supercomputing* (Springer), Vol. 6, No. 1, pp. 71−85, March 1992.

9. S. Weiss, "Optimizing a Superscalar Machine to Run Vector Code," *IEEE Parallel and Distributed Technology*, Vol. 1, No. 2, pp. 73−83, May 1993.

10. S. Weiss and S. Ghahramani, "A Performance Study of Buffered Pseudorandomly Interleaved Memories With Multiple Sections," *Mathematical and Computer Modeling* (Elsevier), Vol. 17, No. 9, pp. 81-87, 1993.

11. S. Weiss, "Increasing the Memory Bandwidth in Superscalar Computers," *Journal of Computer & Software Engineering*, Vol. 1, No. 3, pp. 281−297, 1993.

12. J. E. Smith and S. Weiss, "PowerPC 601 and Alpha 21064: A Tale of Two RISCs," *IEEE Computer*, Vol. 27, No. 6, pp. 46−58, June 1994.

13. S. Reches and S. Weiss, "Implementation and Analysis of Path History in Dynamic Branch Prediction Schemes," *IEEE Transactions on Computers*, Vol. 47, No. 8, pp. 907−912, Aug. 1998.

14. S. Weiss and A. Goldstein, "Floating Point Micropipeline Performance," *Journal of Systems Architecture* (Elsevier), Vol. 45, No. 1, pp. 15 −29, Oct. 1998.

15. S. Weiss and E. Finkelstein, "Extending PCI Performance Beyond the Desktop," *IEEE Computer*, Vol. 32, No. 6, pp. 80−87, June 1999.

16. E. Finkelstein and S. Weiss, "Microprocessor System Buses: A Case Study," *Journal of Systems Architecture* (Elsevier), Vol. 45, No. 12−13, pp. 1151−1168, June 1999.

17. E. Finkelstein and S. Weiss, "Implementation of PCI-based systems using programmable logic," *IEE Proceedings-Circuits, Devices, and Systems* (IEE London), Vol. 147, No. 3, pp. 171−174, June 2000.

18. R. Feig and S. Weiss, "Functional Verification of Instruction Processing Units through Control Flow Modeling," *Microelectronics Journal* (Elsevier), Vol. 33, No. 3, pp. 285 − 299, March 2002.

19. E. Finkelstein and S. Weiss, "A PCI Bus Simulation Framework and Some Simulation Results on the PCI Standard 2.1 Latency Limitations," *Journal of Systems Architecture* (Elsevier), Vol. 47, No. 9, pp. 807−819, March 2002.

20. T. Oved and S. Weiss, "Embedded Instruction Memory in Automotive Engine Controllers," *IEEE Transactions on Vehicular Technology*, Vol. 52, No. 1, pp. 173−183, Jan. 2003.

21. S. Weiss and R. Tsikel, "Approximate Prefix Coding for System-on-a-Chip Programs," *Journal of Systems Architecture* (Elsevier), Vol. 48, No. 13−15, pp. 367 − 375, May 2003.

22. S. Weiss and S. Beren, "Class-Based Decompressor Design for Compressed Instruction Memory in Embedded Processors," *IEEE Transactions on Computers*, Vol. 52, No. 11, pp. 1495−1500, November 2003.

23. T. Karin and S. Weiss, "Programming Windows NT Device Drivers to Operate Non-Interrupting Embedded Devices," *Microprocessors and Microsystems* (Elsevier), Vol. 28, No. 1, pp. 27−35, February 2004.

24. Y. Sadeh Weinraub and S. Weiss, "Power-Aware Out-of-Order Issue Logic in High–Performance Microprocessors," *Microprocessors and Microsystems* (Elsevier), Vol. 30, No. 7, pp. 457−467, 2006.

25. R. Gabor, S. Weiss, and A. Mendelson, "Fairness Enforcement in Switch on Event Multithreading," *ACM Transactions on Architecture and Code Optimization*, Vol. 4, No. 3, pp. 15, Sept. 2007.

26. A. Golander and S. Weiss, "Hiding the Misprediction Penalty of a Resource-Efficient High-Performance Processor," *ACM Transactions on Architecture and Code Optimization*, Vol. 4, No. 4, pp. 6, Jan. 2008.

27. A. Golander, S. Weiss, and R. Ronen, "DDMR: Dynamic and Scalable Dual Modular Redundancy with Short Validation Intervals," *IEEE Computer Architecture Letters*, Vol. 7, 2008.

28. R. Kahn and S. Weiss, "Thrifty BTB: A Comprehensive Solution for Dynamic Power Reduction in Branch Target Buffers," *Microprocessors and Microsystems* (Elsevier), Vol. 32, No. 8, pp. 425−436, November 2008.

29. A. Golander and S. Weiss, "Reexecution and Selective Reuse in Checkpoint Processors," *Transactions on High-Performance Embedded Architectures and Compilers II*, Springer, Lecture Notes in Computer Science, Vol. 5470, pp. 242−268, 2009.

30. A. Golander, S. Weiss, and R. Ronen, "Synchronizing Redundant Cores in a Dynamic DMR Multicore Architecture," *IEEE Transactions on Circuits and Systems II*, Vol. 56, No. 6, pp. 474−478, June 2009.

31. R. Gabor, A. Mendelson, and S. Weiss, "Service Level Agreement for Multithreaded Processors," *ACM Transactions on Architecture and Code Optimization*, Vol. 6, No. 2, pp. 6, June 2009.

32. A. Golander and S. Weiss, "Checkpoint Allocation and Release," *ACM Transactions on Architecture and Code Optimization*, Vol. 6, No. 3, pp. 10, Sept. 2009.

33. R. Kahn and S. Weiss, "Reducing Leakage Power with BTB Access Prediction," *Integration, the VLSI Journal* (Elsevier), Vol. 43, No. 1, pp. 49−57, Jan. 2010.

34. N. Levison and S. Weiss, "Branch Target Buffer Design for Embedded Processors," *Microprocessors and Microsystems* (Elsevier), Vol. 34, No. 6, pp. 215−227, Oct. 2010.

35. G. Motika and S. Weiss, "Virtio network paravirtualization driver: Implementation and performance of a de-facto standard," *Computer Standards & Interfaces* (Elsevier), Vol. 34, No. 1, pp. 36−47, Jan. 2012.

36. N. Cohen and S. Weiss, "Complex Floating Point−A Novel Data Word Representation for DSP Processors," *IEEE Transactions on Circuits and Systems I*, Vol. 59, No. 10, pp. 2252–2262, Oct. 2012.

37. S. Grinberg and S. Weiss, "Architectural Virtualization Extensions: A Systems Perspective," *Computer Science Review* (Elsevier), Vol. 6, No. 5–6, pp. 209−224, Nov. 2012.

38. O. Zilberberg, S. Weiss, and S. Toledo, "Phase Change Memory: An Architectural Perspective," *ACM Computing Surveys*, Vol. 45, No. 3, pp. 29:1-29:33, June 2013.

39. E. Shifer and S. Weiss, "Low-Latency Adaptive Mode Transitions and Hierarchical Power Management in Asymmetric Clustered Cores," *ACM Transactions on Architecture and Code Optimization*, Vol. 10, No. 3, pp. 10:1–10:25, Sept. 2013.

40. G. Oxman, S. Weiss, and Y. Be'ery, "Computational Methods for Conway's Game of Life Cellular Automaton," *Journal of Computational Science* (Elsevier), Vol. 5, No. 1, pp. 24–31, 2014.

41. S. Manole, A. Golander, and S. Weiss, "Protein Sequence Pattern Matching: Leveraging Application Specific Hardware Accelerators," *IEEE Transactions on Computers*, Vol. 63, No. 2, pp. 448–460, Feb. 2014.

42. G. Oxman and S. Weiss, "RIDER: Ring Deflection Router with Buffers," *Design Automation of Embedded Systems* (Springer), Special issue on "On-Chip and Off-Chip Interconnect Architectures," pp. 1–15, Feb. 2014.

43. G. Oxman and S. Weiss, "A simple method to reduce congestion in a bufferless Network-On-Chip," *Electronics Letters* (IET London), Vol. 50, No. 8, pp. 581−583, 10th April 2014.

44. D. Sabo, O. Barzely, S. Weiss, and M. Furst-Yust, "Fast Evaluation of a Time-Domain Non-Linear Cochlear Model on GPUs," *Journal of Computational Physics* (Elsevier), Vol. 265, pp. 97−112, May 2014.

45. A. Jolondz, S. Weiss, and A. Golander, "L1–L2 Interconnect Design Methodology and Arbitration in 3-D IC Multicore Compute Clusters," *IEEE Transactions on VLSI*, Vol. 22, No. 10, pp. 2206−2210, Oct. 2014.

Refereed Articles in Journals — in review

1. Y. Kfir, S. Weiss, and S. Kuschi, "Cloud Computing On Low Bandwidth Airborne Platforms Using Function Based GUI Architecture," submitted to the *IEEE Transactions on Services Computing*, in review.

Refereed Conference Articles

1. R. H. Katz and S. Weiss, "Chip Assemblers: Concepts and Capabilities," *Proceedings 20th ACM/IEEE Design Automation Conferences (DAC '83)*, Miami, Florida, pp. 25−30, June 1983.

2. S. Weiss and J. E. Smith, "Instruction Issue Logic for Pipelined Supercomputers," *Proceedings 11th ACM/IEEE Annual International Symposium on Computer Architecture (ISCA '84)*, Ann Arbor, Michigan, pp. 110−118, June 1984.

   acceptance rate: 39%

3. R. H. Katz and S. Weiss, "Design Transaction Management," *Proceedings 21st ACM/IEEE Design Automation Conference*, Albuquerque, New Mexico, June 1984.

   acceptance rate: 40%

4. S. Weiss, K. Rotzell, T. Rhyne, and A. Goldfein, "DOSS: A Storage System for Design Data," *Proceedings 23rd ACM/IEEE Design Automation Conference (DAC '86)*, Las Vegas, Nevada, pp. 41−47, June 1986.

   acceptance rate: 41%

5. S. Weiss and J. E. Smith, "A Study of Scalar Compilation Techniques for Pipelined Supercomputers," *Proc. 2nd ACM/IEEE Int'l Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS II)*, Palo Alto, Cal., pp. 105−109, Oct. 1987.

   acceptance rate: 34%

6. S. Weiss, "An Aperiodic Storage Scheme to Reduce Memory Conflicts in Vector Processors," *Proceedings 16th ACM/IEEE Annual International Symposium on Computer Architecture (ISCA '89)*, Jerusalem, Israel, pp. 380−385, May 1989.

7. S. Weiss, "Multiple-Port Memory Access in Decoupled Architecture Processors," *Proceedings 20th Int'l Conference on Parallel Processing*, Chicago, Illinois, pp. I-373 − I-376, August 1991.

8. S. Weiss, "Implementing Register Interlocks in Parallel Pipeline, Multiple Instruction Queue, Superscalar Processors," *First IEEE International Symposium on High−Performance Computer Architecture (HPCA '95)*, Raleigh, North Carolina, pp. 14−21, Jan. 1995.

   acceptance rate: 19%

9. S. Reches and S. Weiss, "Implementation and Analysis of Path History in Dynamic Branch Prediction Schemes," *Proceedings 11th ACM International Conference on Supercomputing (ICS '97)*, Vienna, Austria, pp. 285−292, July 1997.

   acceptance rate: 33%

10. D. Zeevi and S. Weiss, "Performance of DSP Applications Using Intel's Multimedia Instruction Set Extensions," *Proceedings 1998 IEEE International Conference and Workshop on Engineering of Computer Based Systems*, Jerusalem, Israel, pp. 174−178, March 1998.

11. E. Federovsky, M. Feder, and S. Weiss, "Branch Prediction Based on Universal Data Compression Algorithms," *Proceedings 25th ACM/IEEE Annual International Symposium on Computer Architecture (ISCA '98)*, Barcelona, Spain, June 1998.

12. S. Weiss and S. Beren, "HW/SW Partitioning of an Embedded Instruction Memory Decompressor," *Proceedings 9th ACM/IEEE Int'l Hardware/Software Codesign Symposium (CODES '01)*, Copenhagen, Denmark, pp. 36−41, April 2001.

    acceptance rate: 28%

13. A. Orpaz and S. Weiss, "A Study of CodePack: Optimizing Embedded Code Space," *Proceedings 10th ACM/IEEE Int'l Hardware/Software Codesign Symposium (CODES '02)*, Estes Park, Colorado, pp. 103−108, May 2002.

    acceptance rate: 33%

14. R. Gabor, S. Weiss, and A. Mendelson, "Fairness and Throughput in Switch on Event Multithreading," *Proceedings 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO '06)*, Orlando, Florida, pp. 149−160, Dec. 2006.

    acceptance rate: 24%

15. N. Levison and S. Weiss, "Low Power Branch Prediction for Embedded Application Processors," *Proceedings 16th IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED '10)*, Austin, Texas, pp. 67−72, August 2010.

    acceptance rate: 34%

16. G. Oxman, S. Weiss, and Y. Birk, "Streamlined Network-on-Chip for Multicore Embedded Architectures," *Proceedings of the 2012 Int'l Conference on Architecture of Computing Systems (ARCS 2012)*, Springer, LNCS 7179, pp. 238−249, Munich, Germany, March 2012.

    acceptance rate: 31%

17. D. Sabo, S. Weiss, and M. Furst-Yust, "A Parallel Algorithm for a Physiological Non-Linear Model of the Cochlea," *Proceedings of the 2013 International Conference on Computational Science (ICCS 2013)* Elsevier, Procedia Computer Science, Vol. 18, pp. 682−691, Barcelona, Spain, June 2013.

18. E. Shifer and S. Weiss, "Low-Latency Adaptive Mode Transitions and Hierarchical Power Management in Asymmetric Clustered Cores," published in the *ACM Transactions on Architecture and Code Optimization (TACO)* (see item 39 in Journal publications), presented at the High-Performance Embedded Architectures and Compilers (HiPEAC) Conference, Vienna, Austria, January 2014.

19. G. Oxman and S. Weiss, "DNOC: An Accurate and Fast Virtual Channel and Deflection Routing Network-On-Chip Simulator," accepted for publication in the *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2015)*, Philadelphia, Pennsylvania, March 2015.

    acceptance rate: 33%

Unrefereed Conference and Workshop Articles and Poster

1. S. Weiss and R. H. Katz, "Recovery of In-Memory Data Structures for Interactive Update Applications," *Proceedings 28th IEEE Computer Society International Conference*, San Francisco, California, February 1984.

2. A. Goldstein and S. Weiss, "ePASS−A Software Based POWER Simulator," *7th IEEE Israeli Conf. on Computer Systems and Software Engineering*, Herzliya, Israel, pp. 46-54, June 1996.

3. A. Besserglik and S. Weiss, "Implementation and Bandwidth Considerations in Multiported On-Chip Data Caches," *Proceedings IEEE 19th Convention of Electrical and Electronics Engineers in Israel*, Jerusalem, Israel, pp. 152−155, Nov. 1996.

4. E. Finkelstein and S. Weiss, "PCI Interface Implementation Using CPLD and FPGA Devices," *Proceedings 9th IEEE Mediterranean Electrotechnical Conference (Melecon '98)*, Tel-Aviv, Israel, pp. 1284−1287, May 1998.

5. T. Karin and S. Weiss, "Programming Windows NT Device Drivers to Operate Non-Interrupting Embedded Devices," *Proceedings IEEE 22nd Convention of Electrical and Electronics Engineers in Israel*, Jerusalem, Israel, pp. 105−107, Dec. 2002.

6. A. Orpaz and S. Weiss, "Pattern Matching by means of Multi-Resolution Compression," *Proceedings IEEE Data Compression Conference* (poster presentation), Snowbird, Utah, p. 441, March 2003.

7. D. Nakar and S. Weiss, "Selective Main Memory Compression by Identifying Program Phase Changes," *Proceedings of the Third Workshop on Memory Performance Issues (WMPI '04), held in conjunction with the 31st ACM/IEEE International Symposium on Computer Architecture (ISCA)*, Munich, Germany, pp. 96−101, June 2004.

8. S. Grinberg and S. Weiss, "Investigation of Transactional Memory Using FPGAs," *Proceeding 24th IEEE Convention of Electrical and Electronics Engineers in Israel*, pp. 119−122, November 2006.

9. S. Manole, A. Golander, and S. Weiss, "Workload Optimization of Proteomics Pattern Matching Using Embedded Accelerator," *Proceedings 26th IEEE Convention of Electrical and Electronics Engineers in Israel (IEEEI '10)*, Eilat, Israel, pp. 790−794, Nov. 2010.

10. G. Oxman, S. Weiss, and Y. Birk, "Buffered Deflection Routing for Networks-on-Chip," *Proceedings of the Interconnection Network Architecture: On-Chip, Multi-Chip Workshop (INA-OCMC '12)*, held in conjunction with the 7th HiPEAC Conference, pp. 9−12, Paris, France, Jan. 2012.

11. S. Kushchi, Y. Kfir, and S. Weiss, "Cloud Computing Through Limited Bandwidth Inflight Airplane WiFi Communication," *Proceedings 28th IEEE Convention of Electrical and Electronics Engineers in Israel (IEEEI '14)*, Eilat, Israel, Dec. 2014.

12. L. Ainey, A. Efrati, and S. Weiss, "Parallel Cycle-Accurate System C kernel," *Proceedings 28th IEEE Convention of Electrical and Electronics Engineers in Israel (IEEEI '14)*, Eilat, Israel, Dec. 2014.