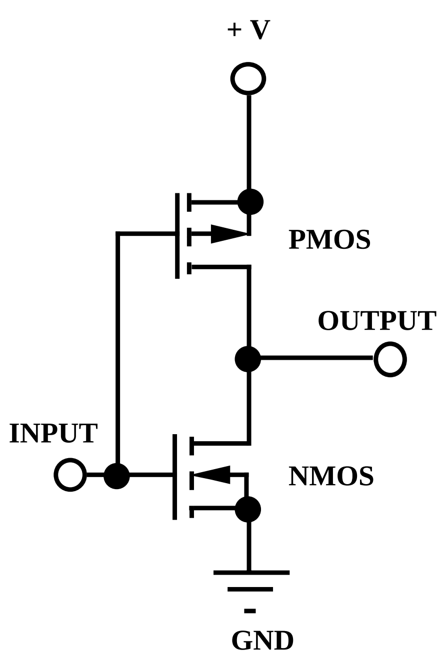
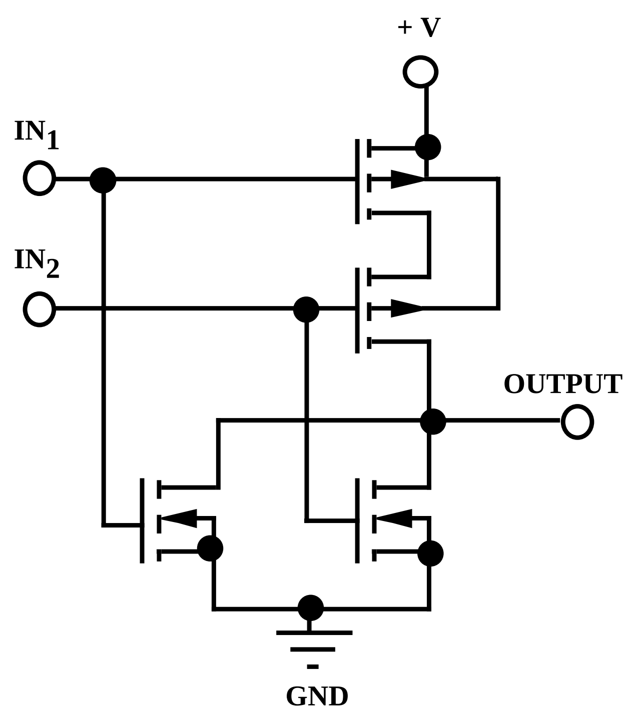
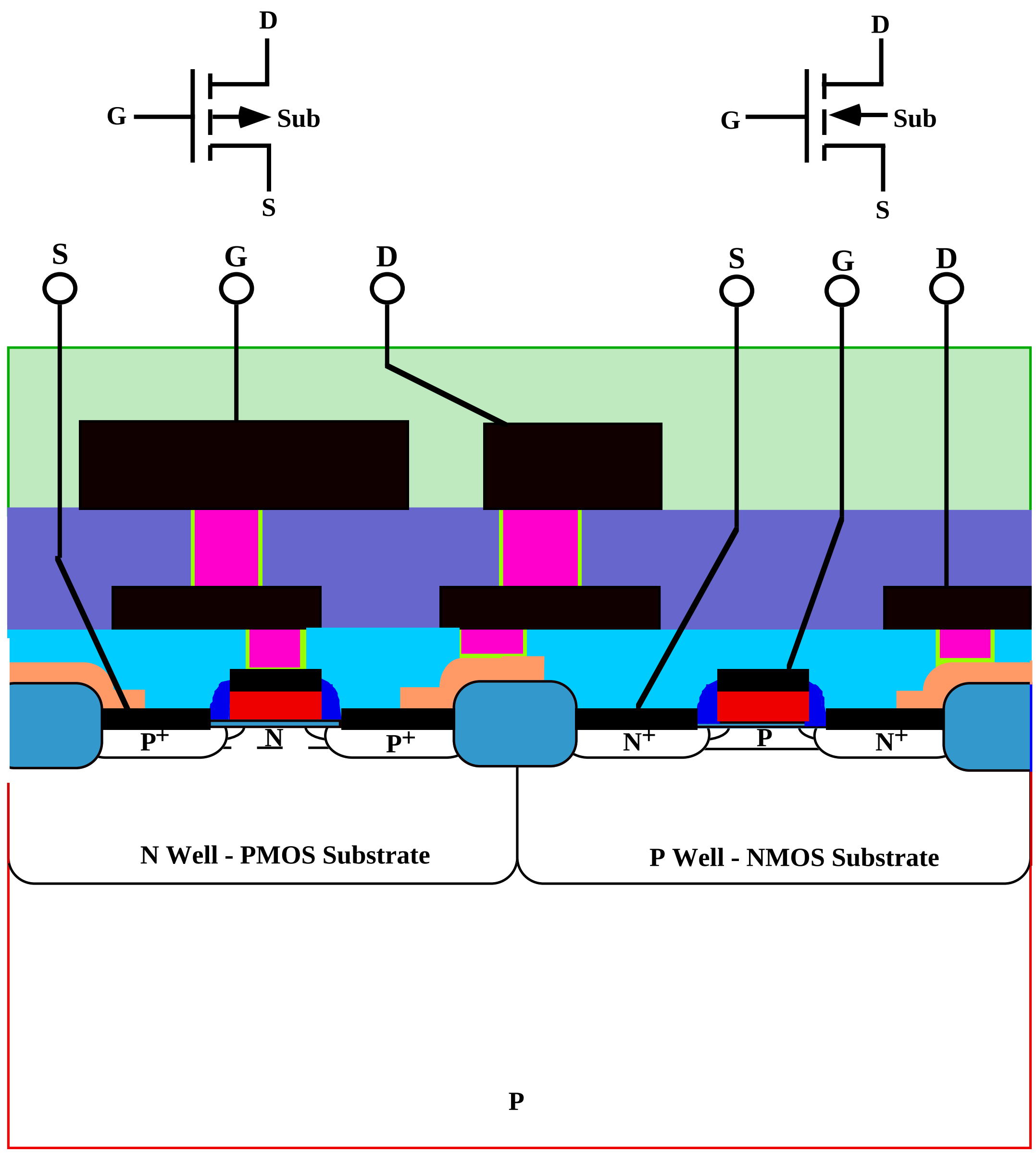
CMOS TECHNOLOGY- Chapter 2 in the Text

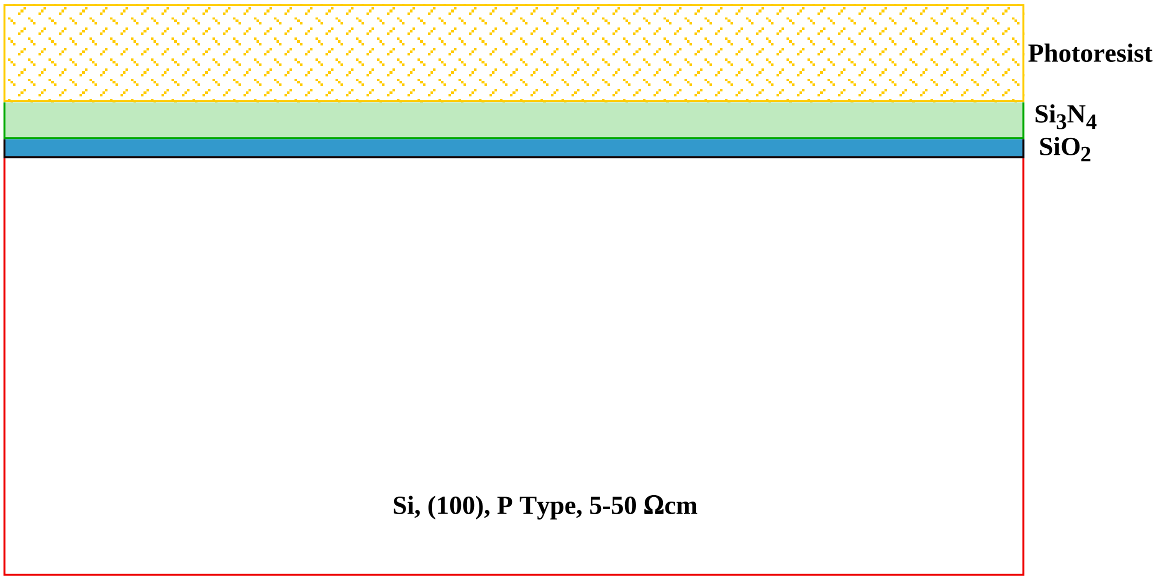
- We will describe a modern CMOS process flow.
- In the simplest CMOS technologies, we need to realize simply NMOS and PMOS transistors for circuits like those illustrated below.
- Typical CMOS technologies in manufacturing today add additional steps to implement multiple device V_{TH}, TFT devices for loads in SRAMs, capacitors for DRAMs etc.
- Process described here will require 16 masks (through metal 2) and > 100 process steps.
- There are many possible variations on the process flow described here, some of which are described in Chapter 2 in the text. See the STI section in the text especially.



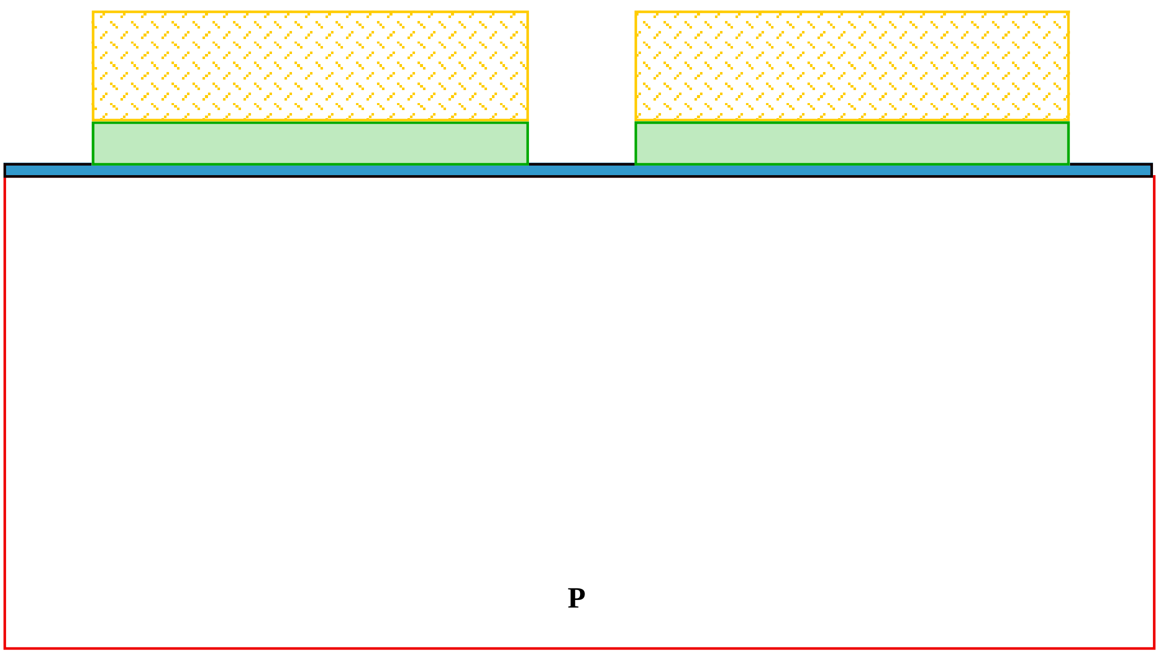




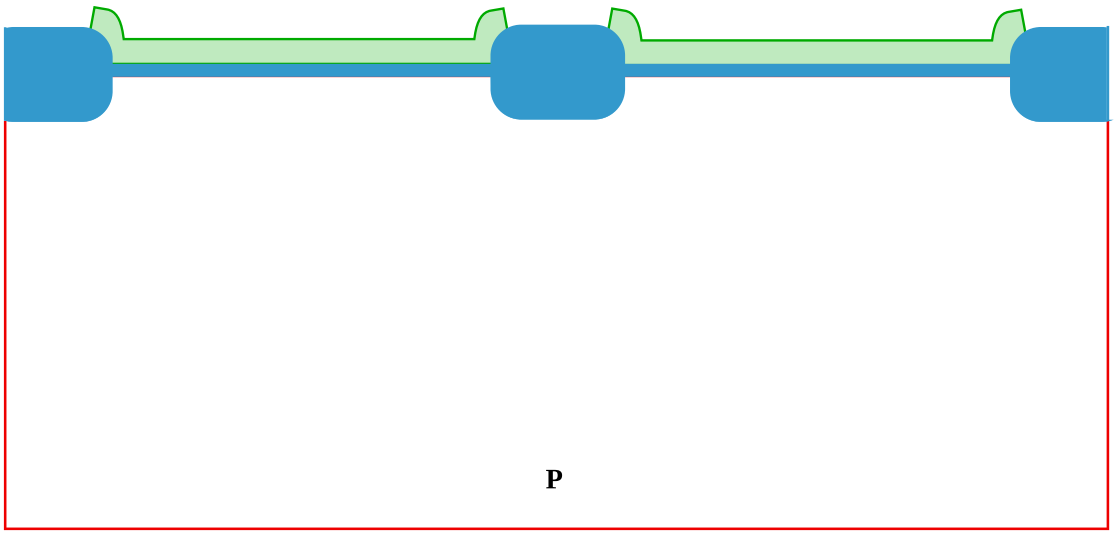
• **Final result of the process flow we will consider.**



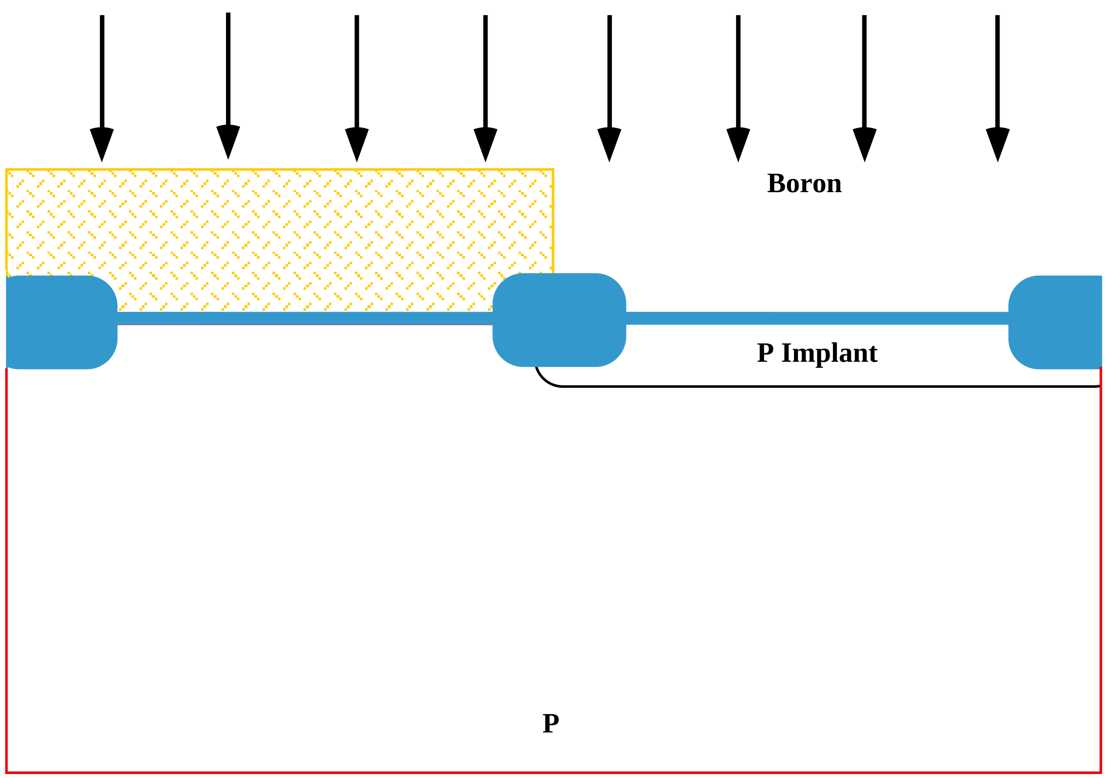
- **Substrate selection: moderately high resistivity, (100) orientation, P type.**
- **Wafer cleaning, thermal oxidation (≈ 40 nm), nitride LPCVD deposition (≈ 80 nm), photoresist spinning and baking (≈ 0.5 - 1.0 µm).**



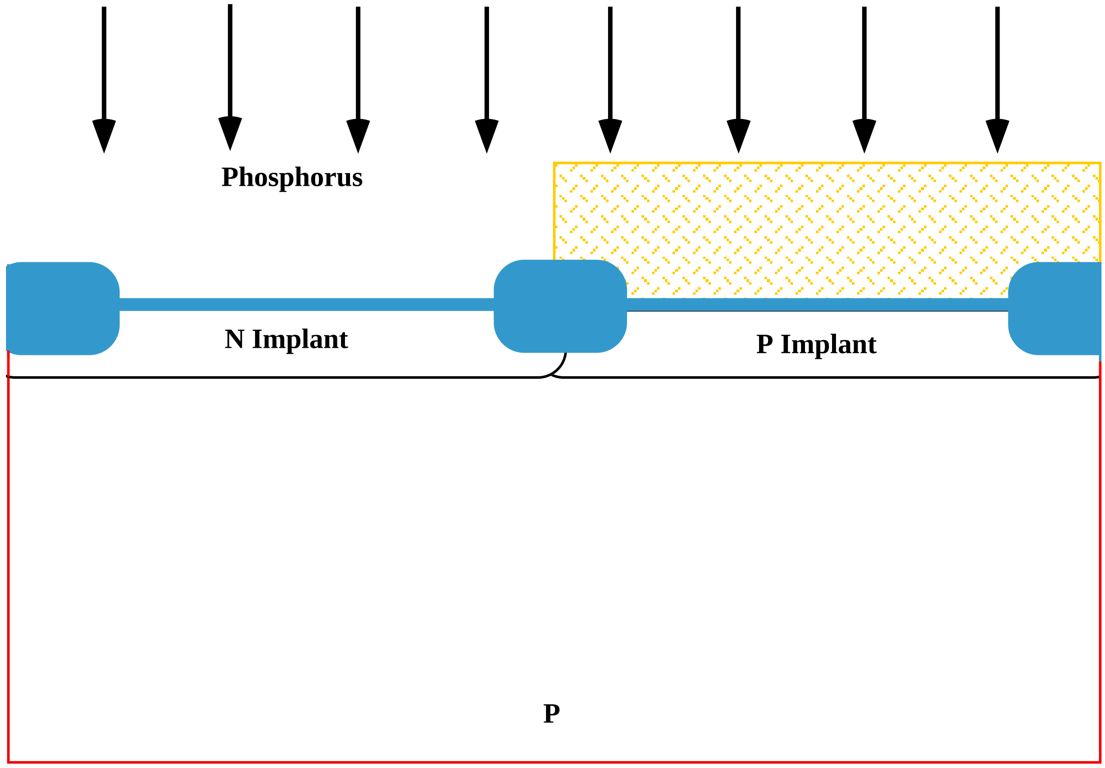
- **Mask #1 patterns the active areas. The nitride is dry etched.**



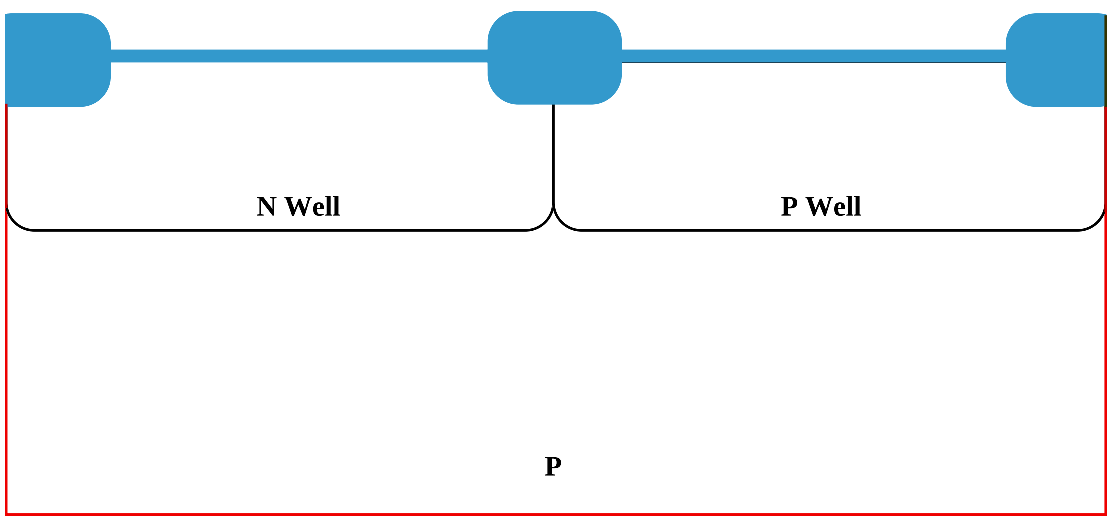
- **Field oxide is grown using a LOCOS process. Typically 90 min @ 1000 ˚C in H_2O grows ≈ 0.5 µm.**



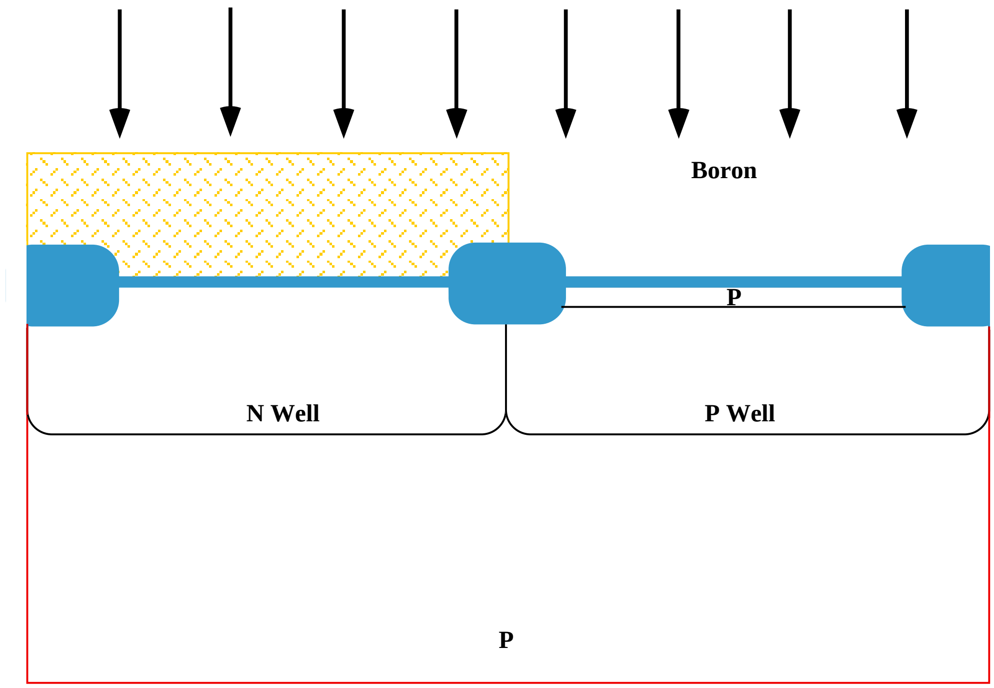
- **Mask #2 blocks a B^+ implant to form the wells for the NMOS devices. Typically 10^{13} cm^{-2} @ 150-200 KeV.**



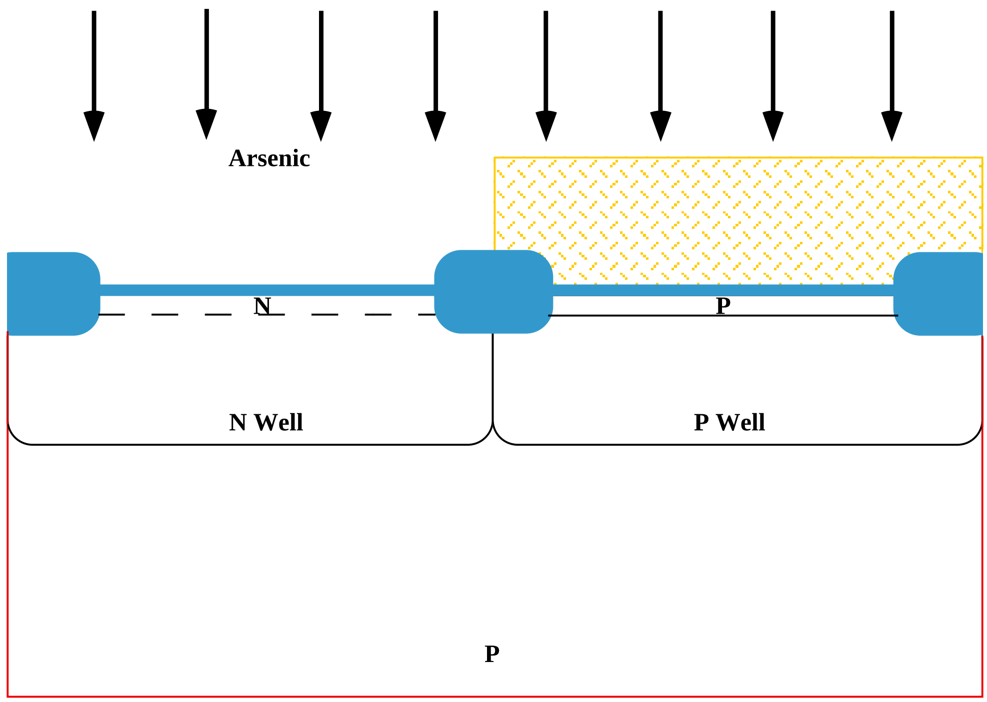
• **Mask #3 blocks a P^+ implant to form the wells for the PMOS devices. Typically 10^{13} cm^{-2} @ 300^+ KeV.**



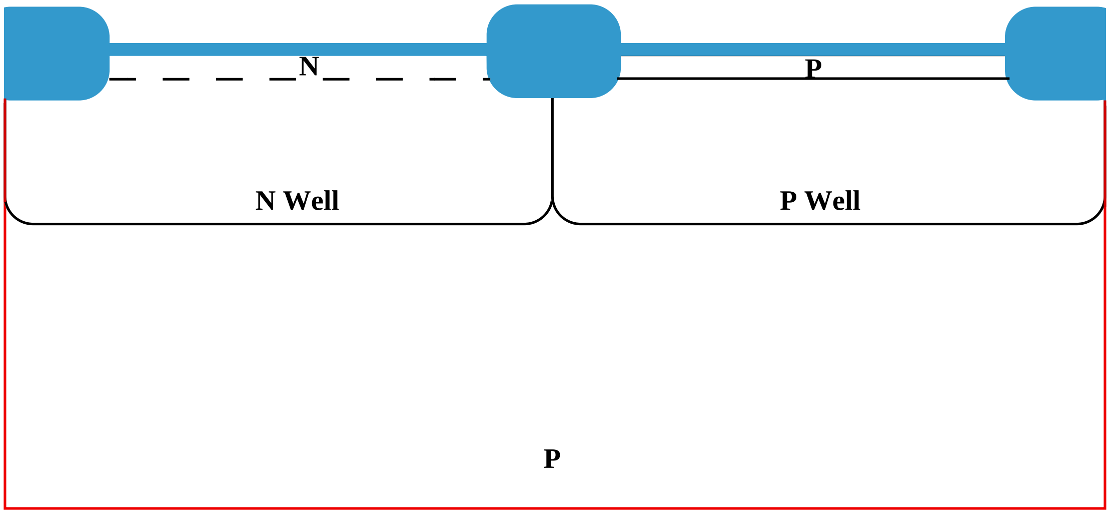
• **A high temperature drive-in produces the "final" well depths and repairs implant damage. Typically 4-6 hours @ 1000 ˚C - 1100 ˚C or equivalent Dt.**



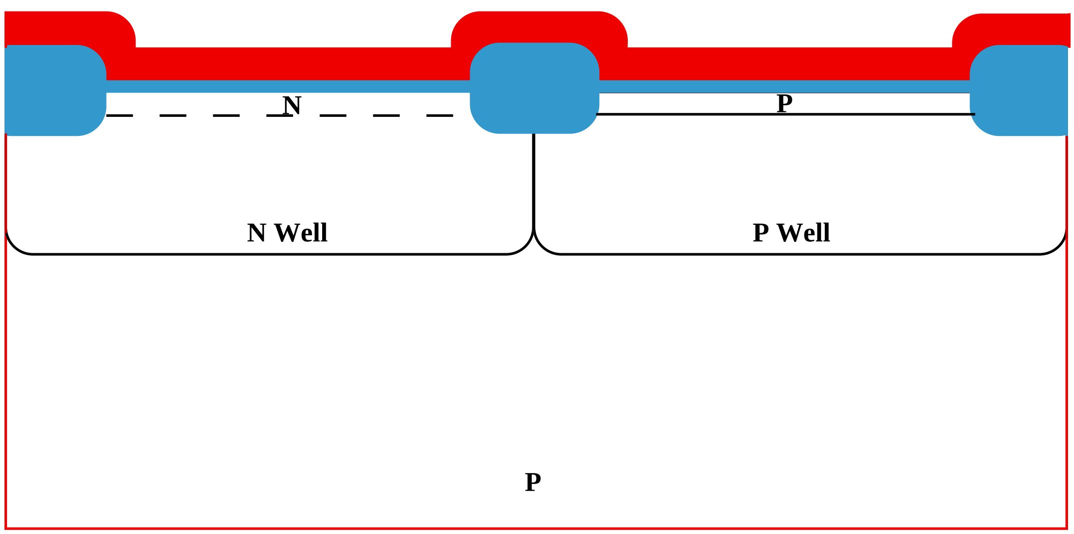
- **Mask #4 is used to mask the PMOS devices. A V_{TH} adjust implant is done on the NMOS devices, typically a 1-5 x 10^{12} cm^{-2} B^{+} implant @ 50 - 75 KeV.**



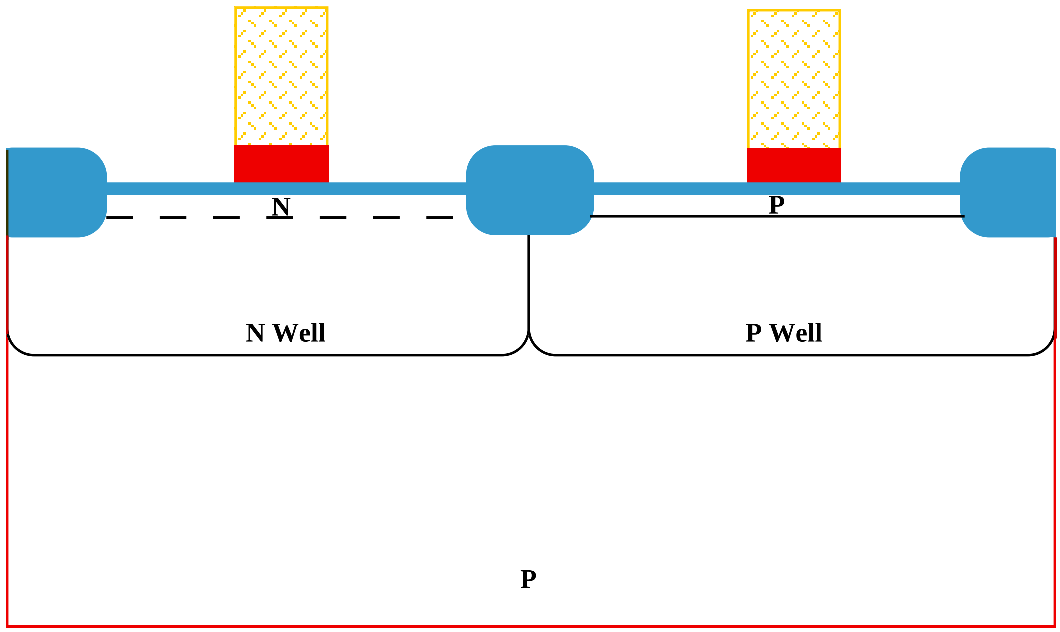
- **Mask #5 is used to mask the NMOS devices. A V_{TH} adjust implant is done on the PMOS devices, typically 1-5 x 10^{12} cm^{-2} As^{+} implant @ 75 - 100 KeV.**



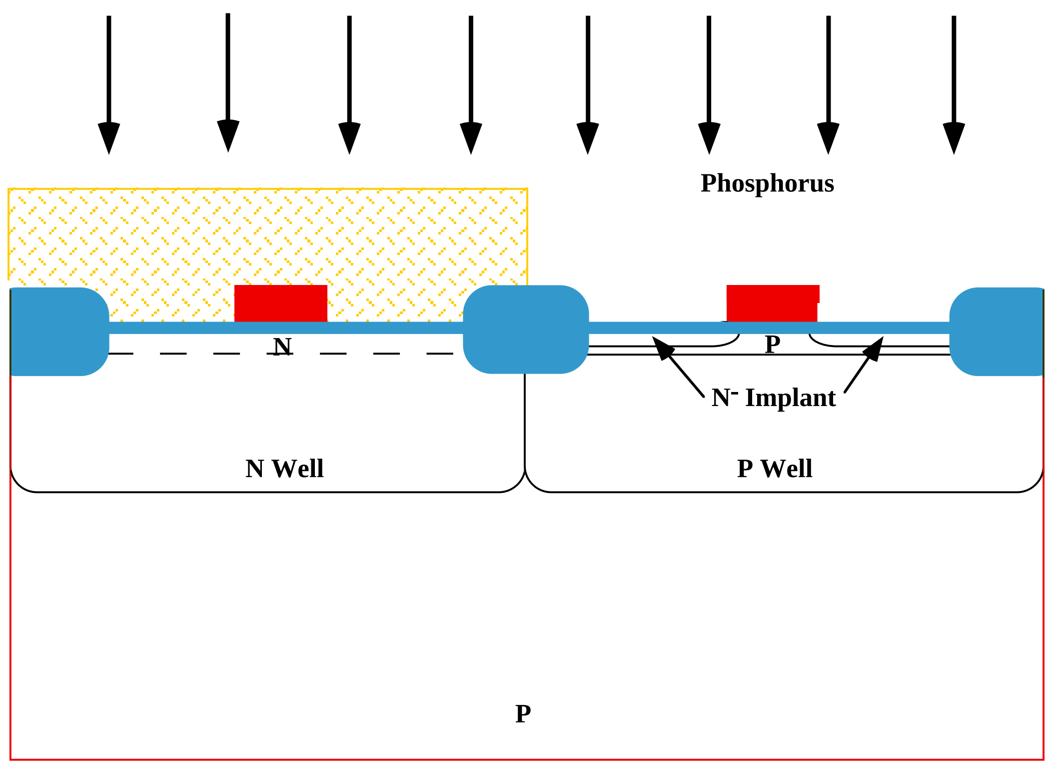
- **The thin oxide over the active regions is stripped and a new gate oxide grown, typically 3 - 5 nm, which could be grown in 0.5 - 1 hrs @ 800 ˚C in O_2.**



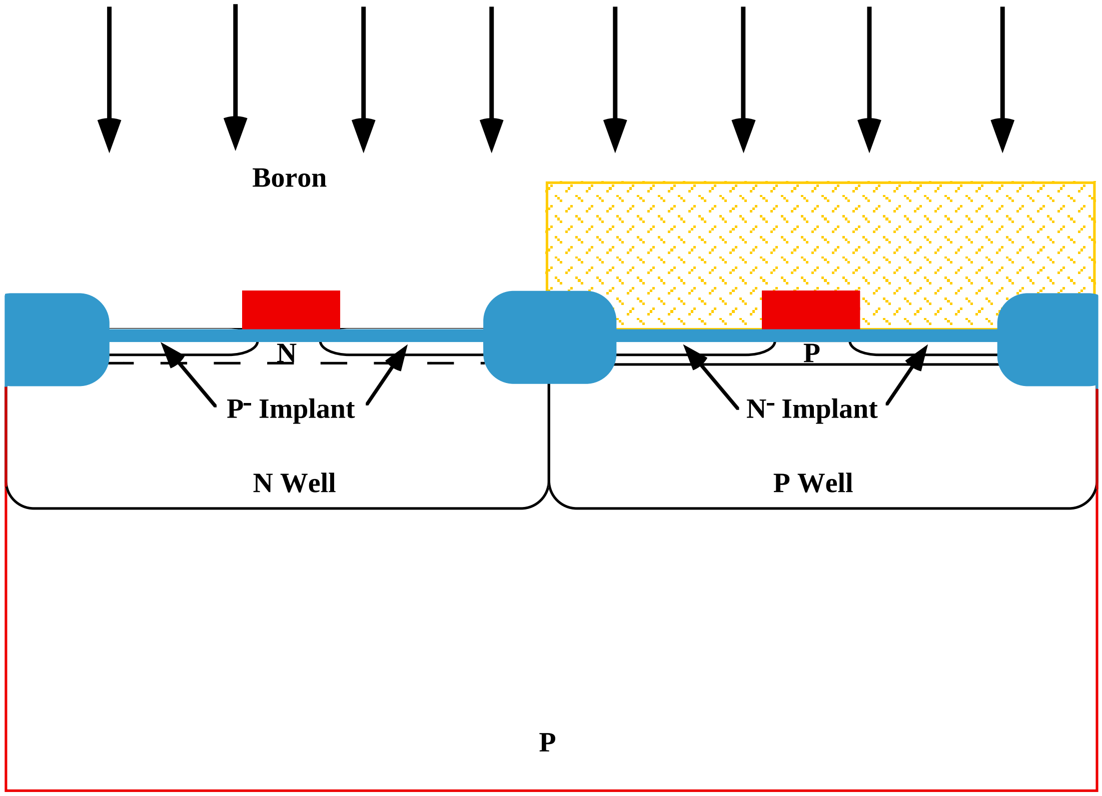
- **Polysilicon is deposited by LPCVD (≈ 0.5 µm). An unmasked P^+ or As^+ implant dopes the poly (typically 5×10^{15} cm^{-2}).**



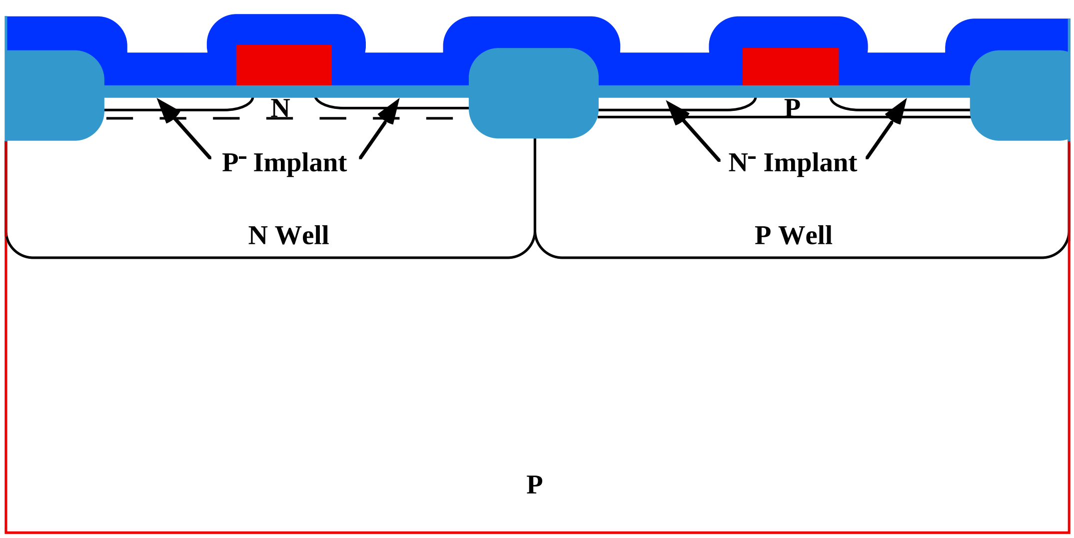
- Mask #6 is used to protect the MOS gates. The poly is plasma etched using an anisotropic etch.



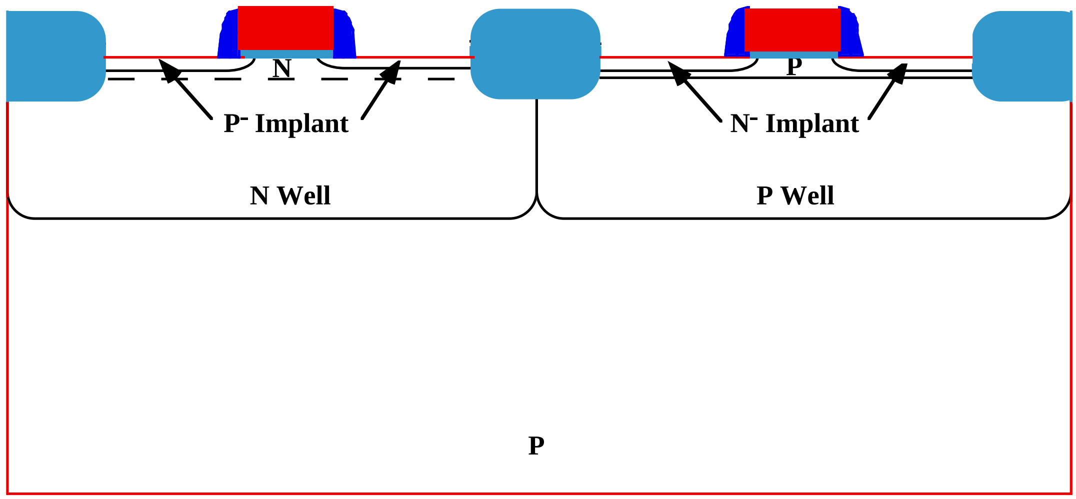
- Mask #7 protects the PMOS devices. A P^+ implant forms the LDD regions in the NMOS devices (typically 5×10^{13} cm^{-2} @ 50 KeV).



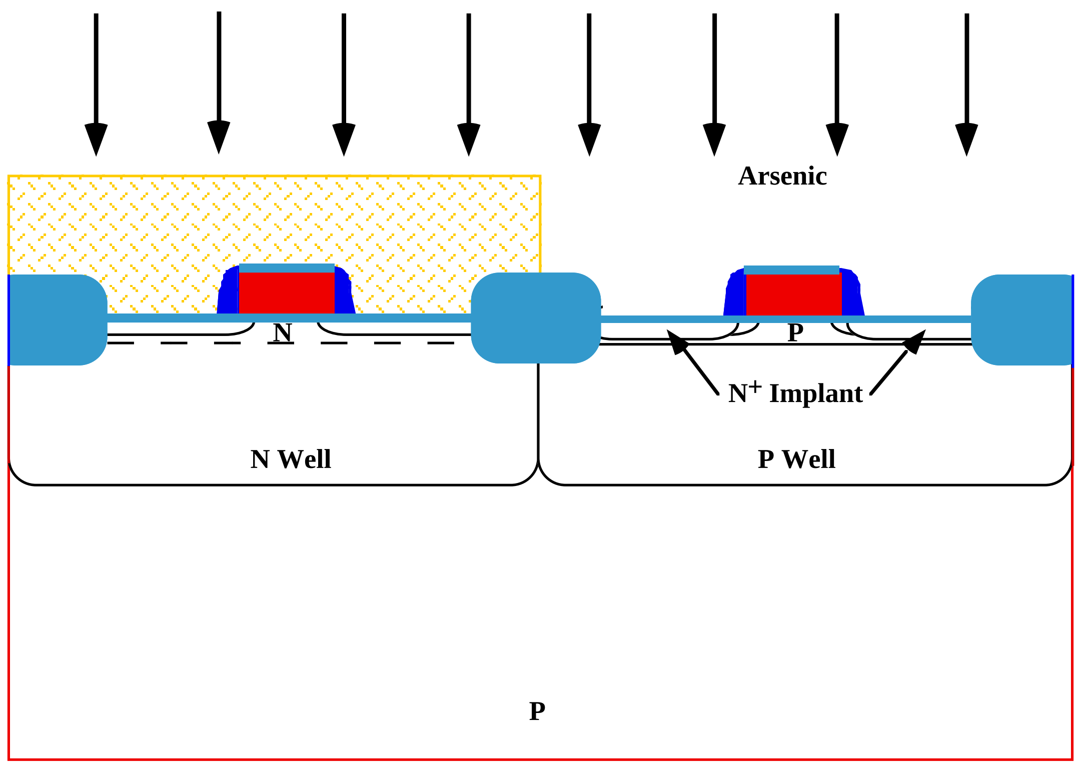
• Mask #8 protects the NMOS devices. A B^+ implant forms the LDD regions in the PMOS devices (typically 5×10^{13} cm^{-2} @ 50 KeV).



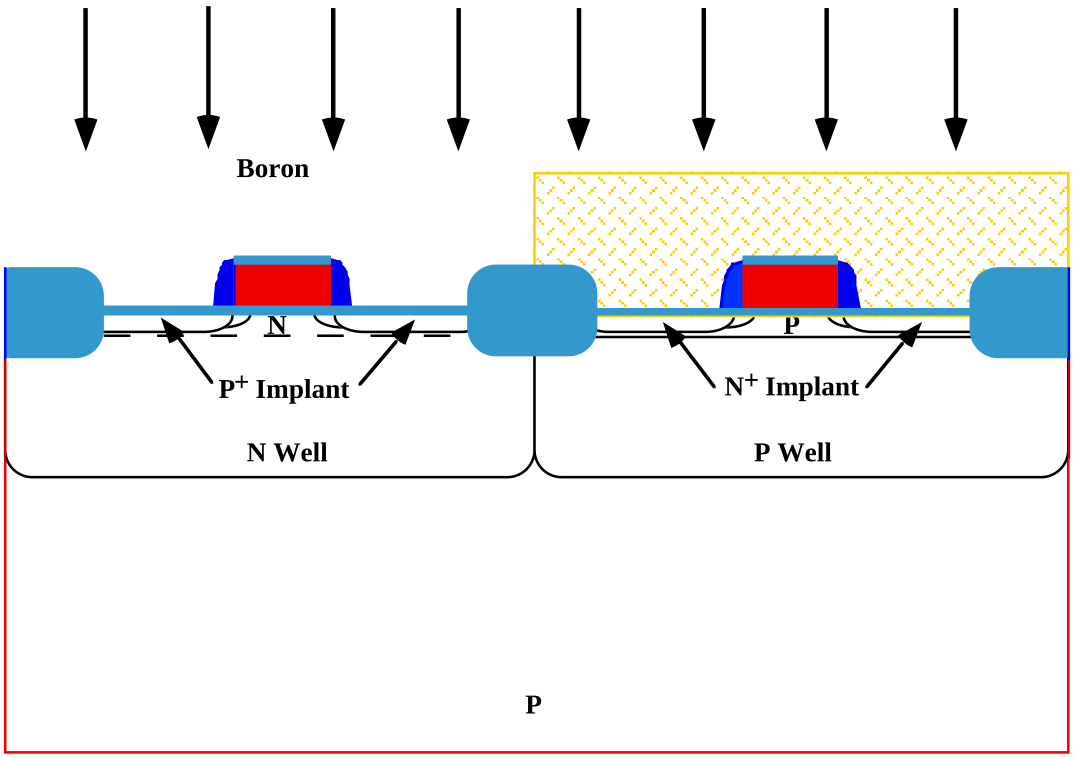
• Conformal layer of SiO_2 is deposited (typically 0.5 µm).



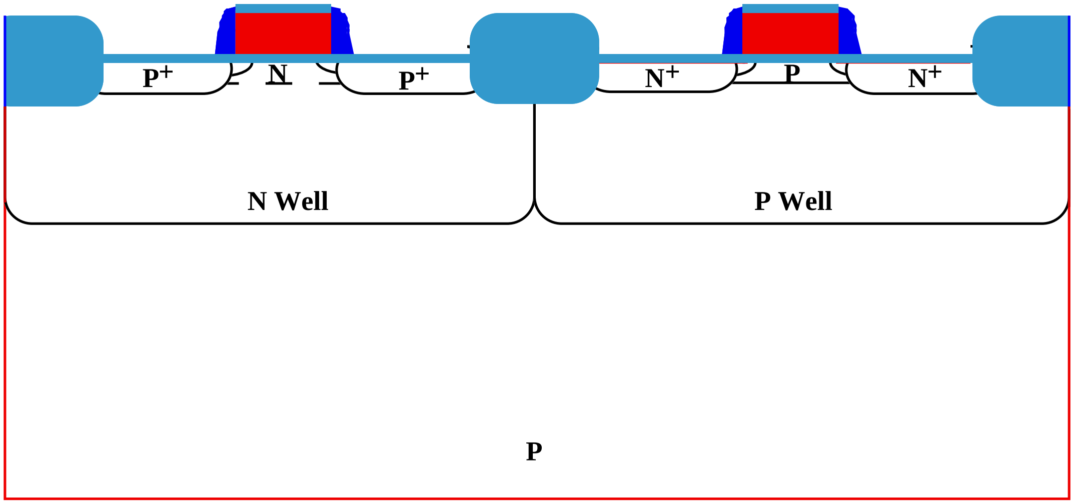
• **Anisotropic etching leaves "sidewall spacers" along the edges of the poly gates.**



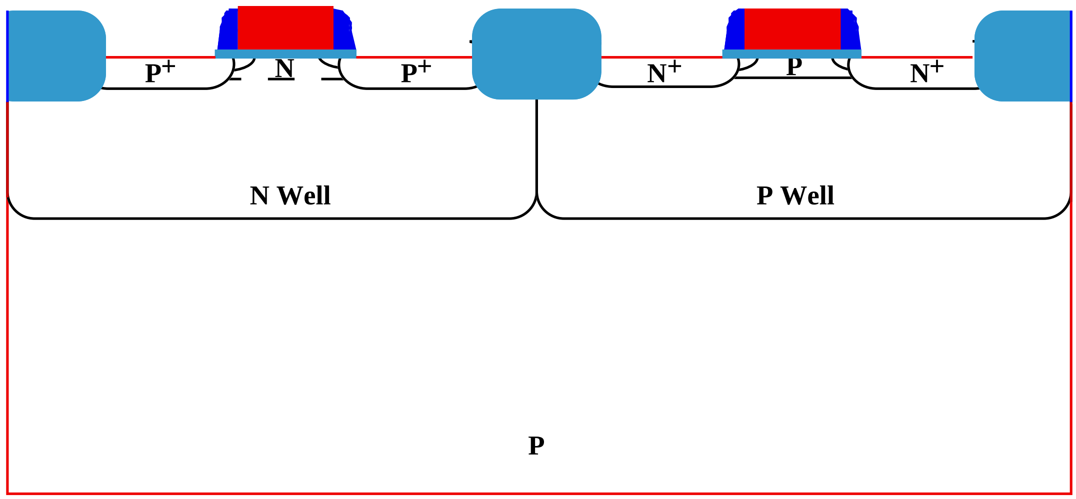
• **Mask #9 protects the PMOS devices, An As^+ implant forms the NMOS source and drain regions (typically 2-4 x 10^{15} cm^{-2} @ 75 KeV).**



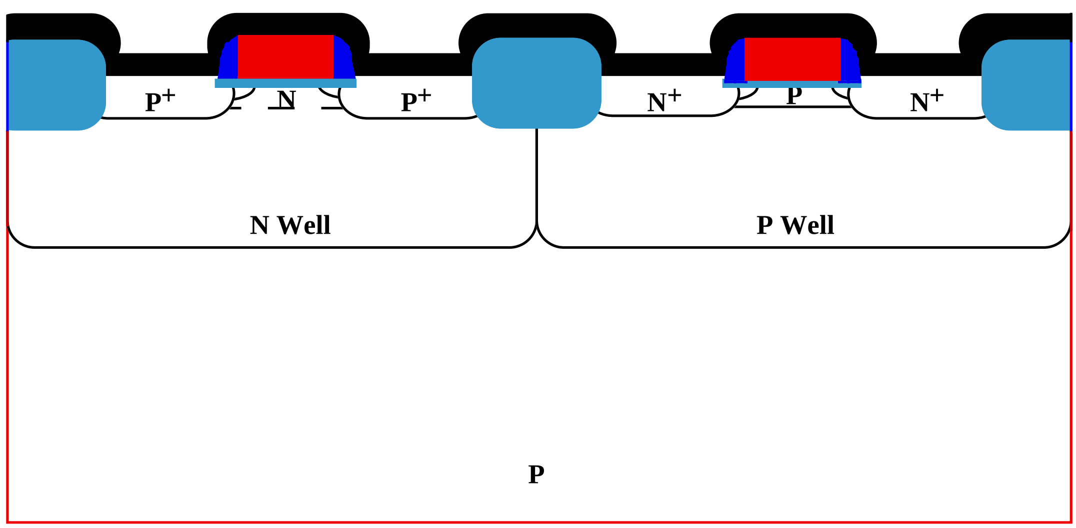
• **Mask #10 protects the NMOS devices, A B^+ implant forms the PMOS source and drain regions (typically 1-3 x 10^{15} cm^{-2} @ 50 KeV).**



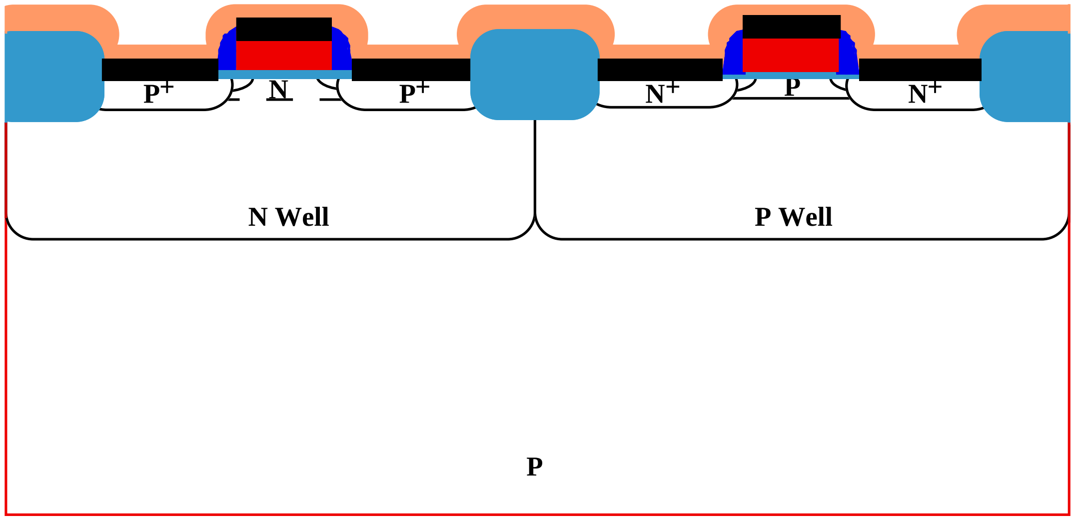
• **A final high temperature anneal drives-in the junctions and repairs implant damage (typically 30 min @ 900 ˚C or 1 min RTA @ 1000 ˚C).**



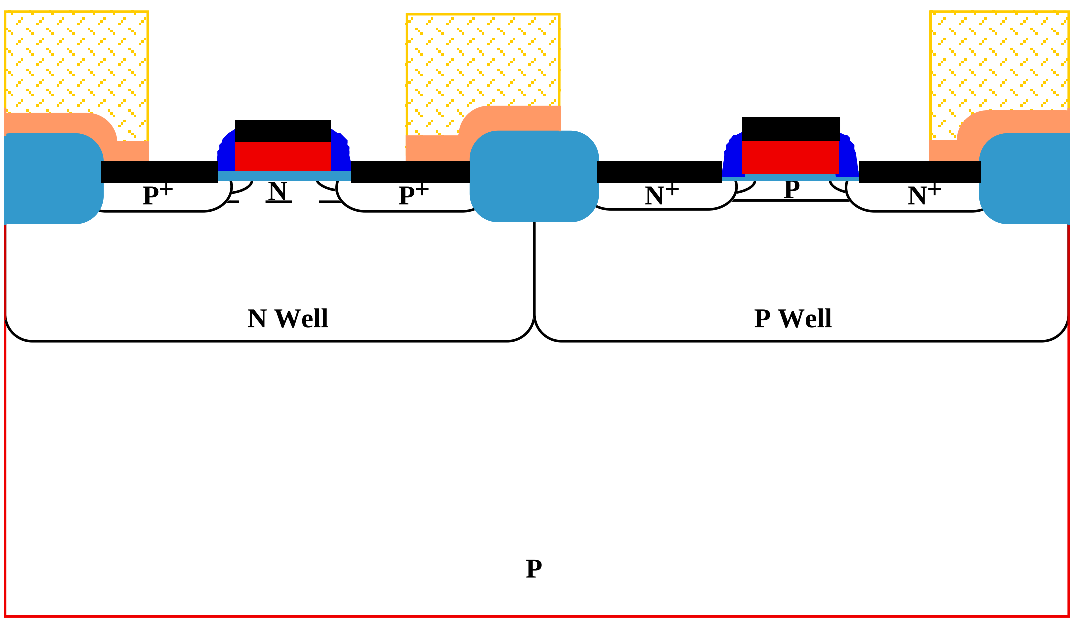
• **An unmasked oxide etch allows contacts to Si and poly regions.**



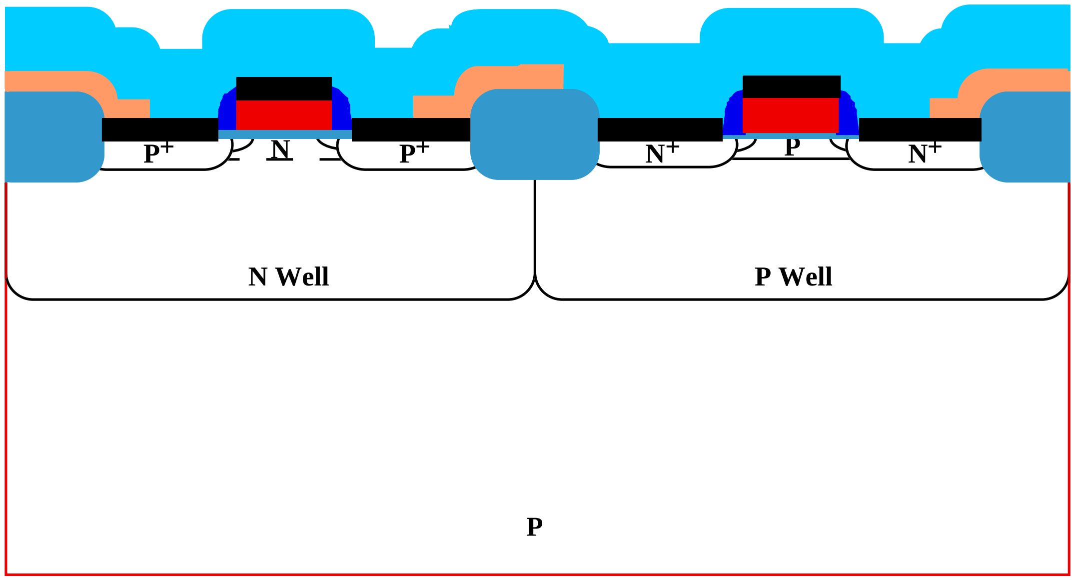
• **Ti is deposited by sputtering (typically 100 nm).**



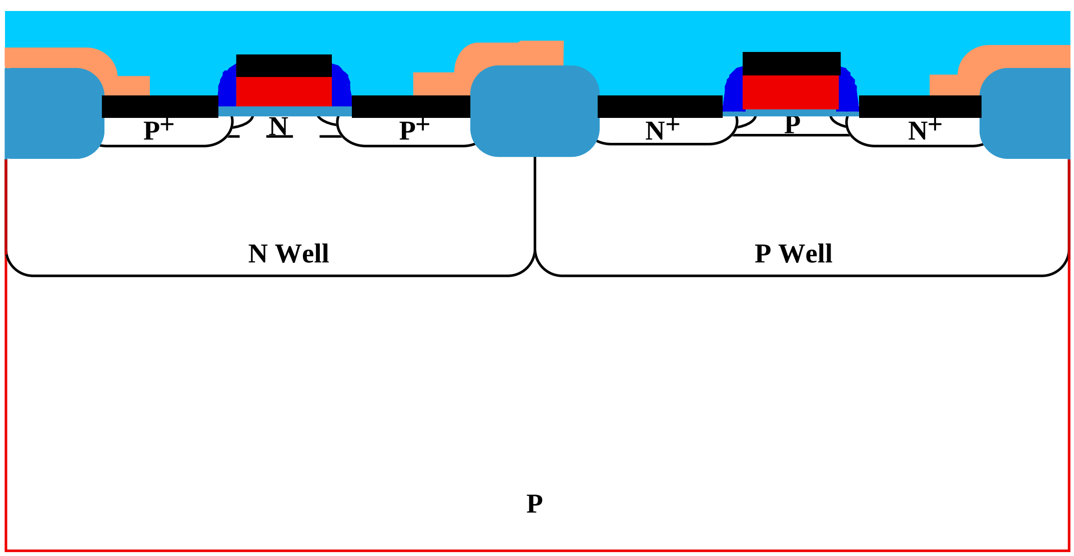
- The Ti is reacted in an N_2 ambient, forming $TiSi_2$ and TiN (typically 1 min @ 600 - 700 ˚C).



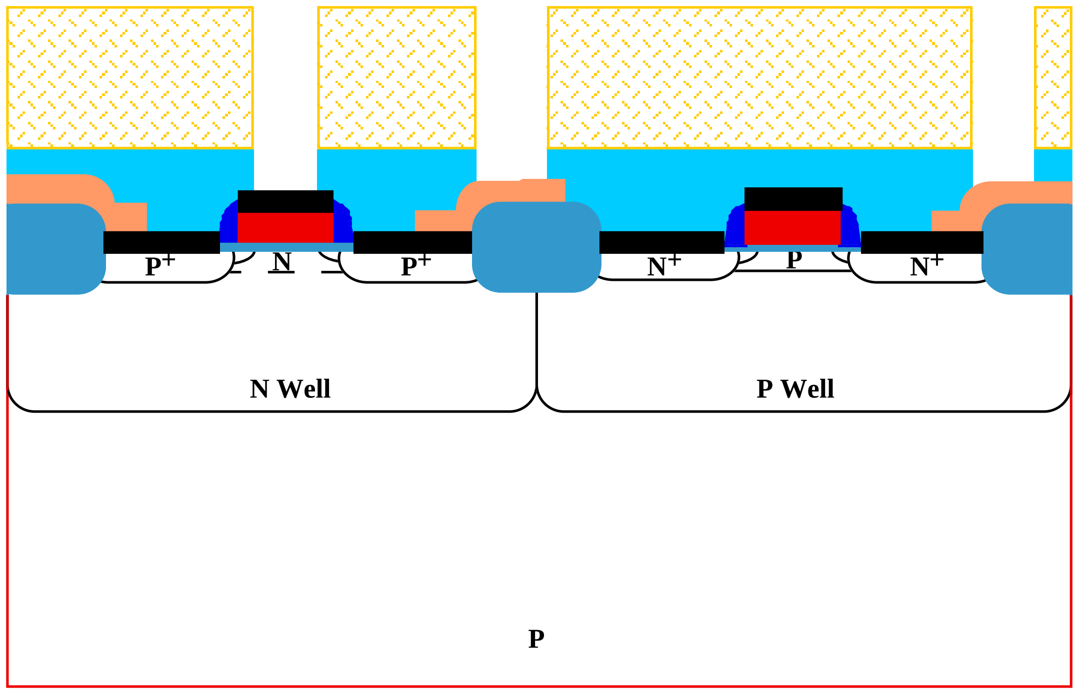
- Mask #11 is used to etch the TiN, forming local interconnects.



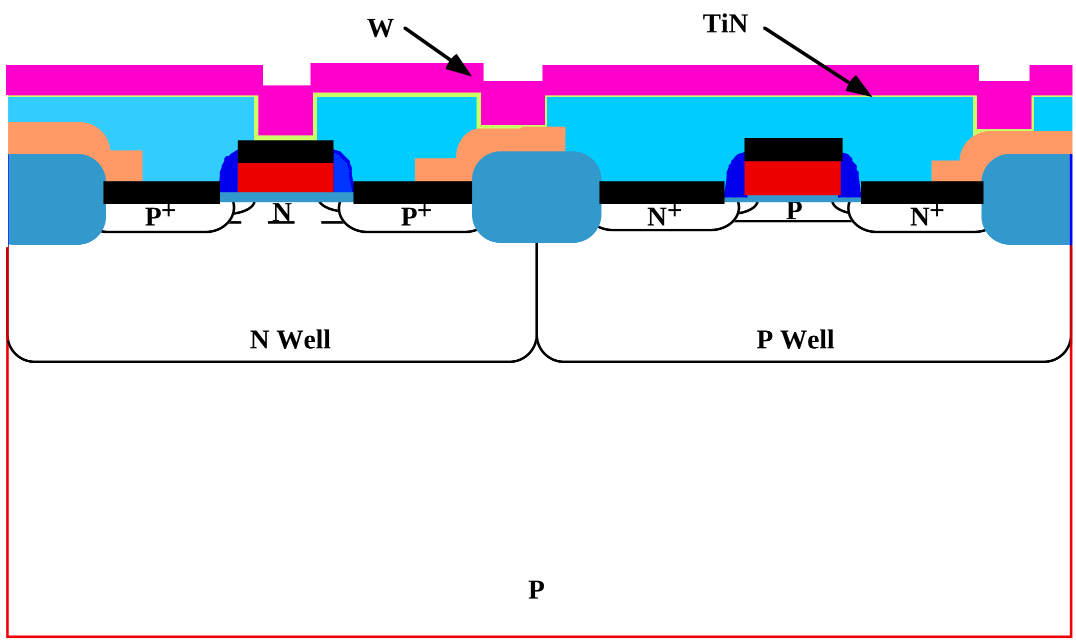
• **A conformal layer of SiO_2 is deposited by LPCVD (typically 1 µm).**



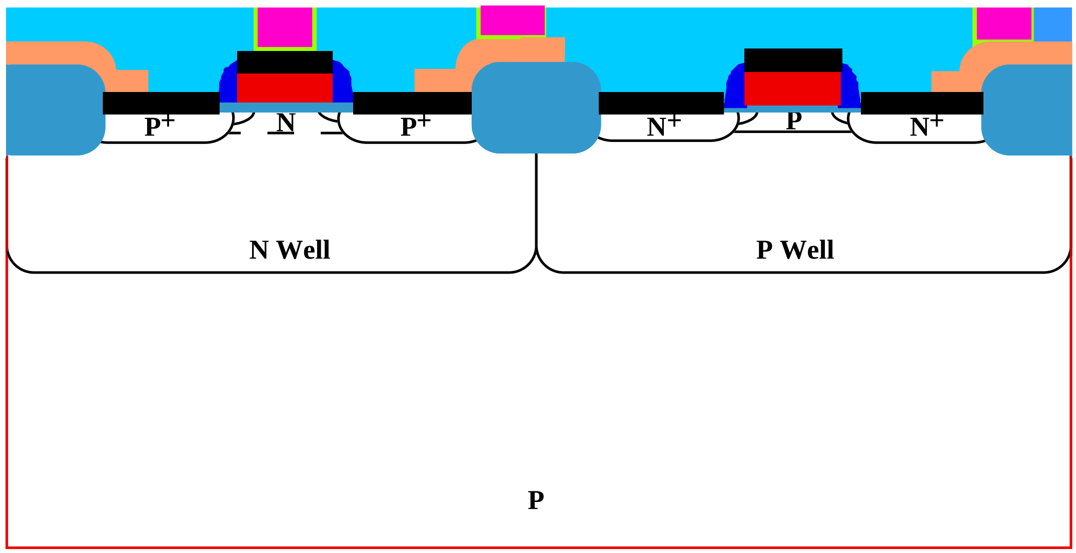
• **CMP is used to planarize the wafer surface.**



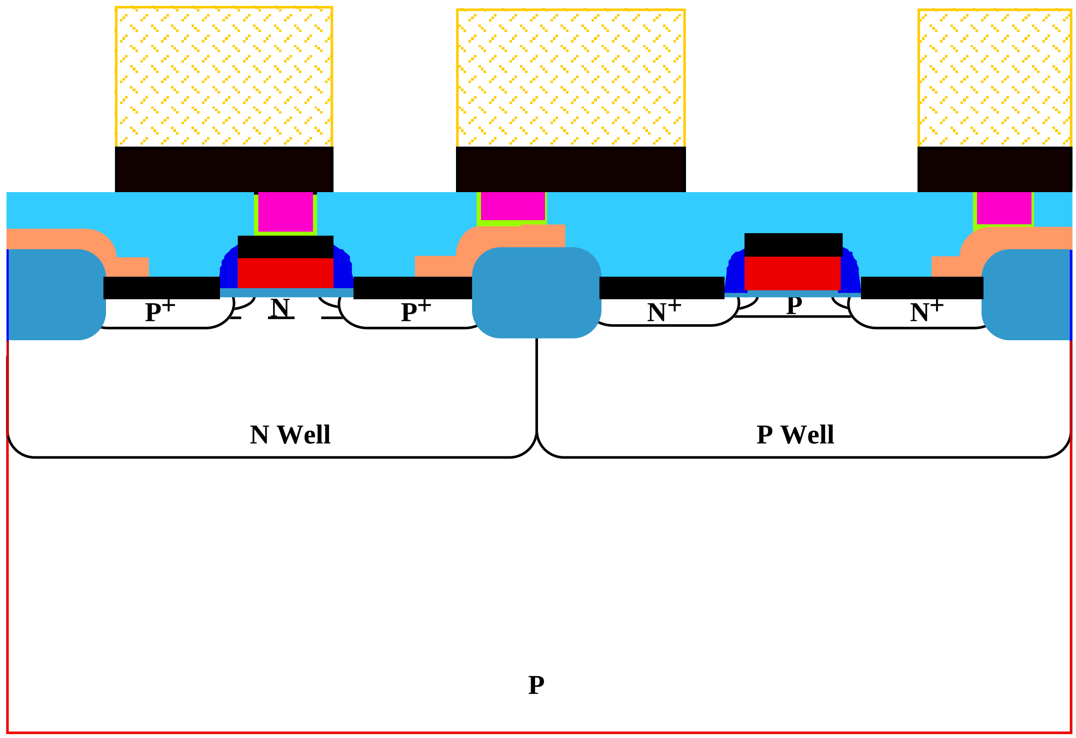
• Mask #12 is used to define the contact holes. The SiO_2 is etched.



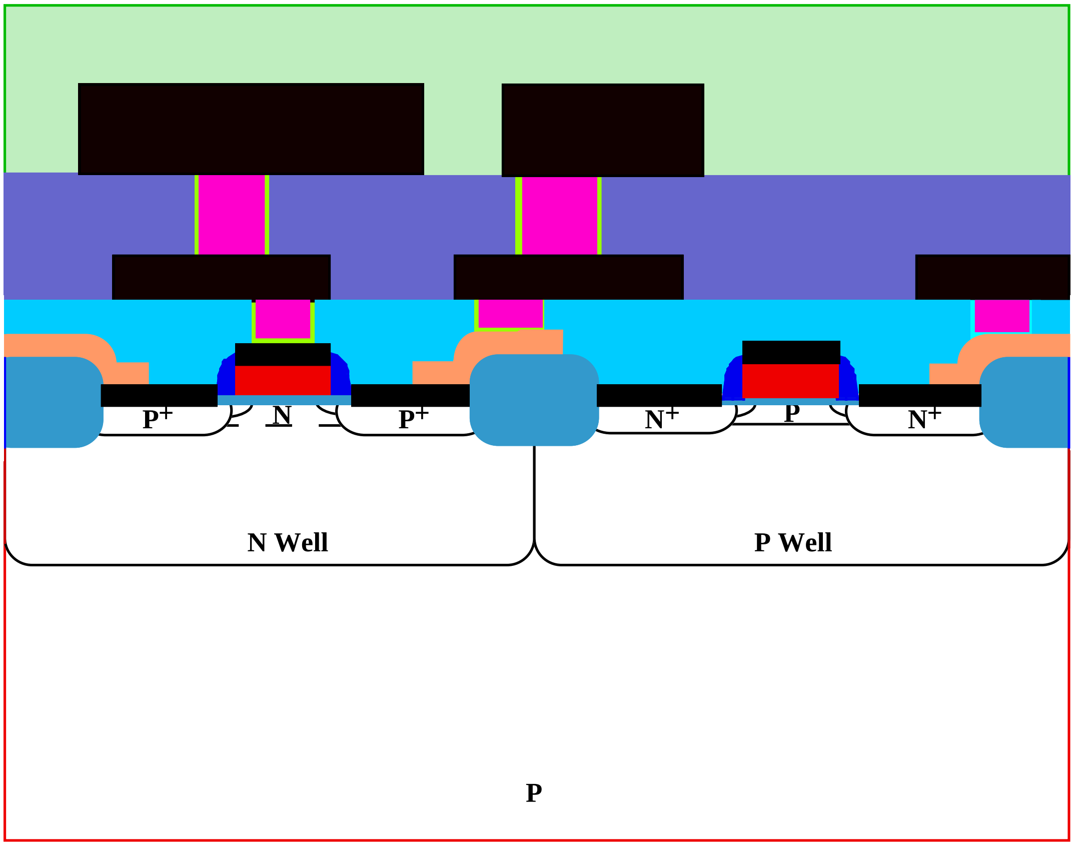
• A thin TiN barrier layer is deposited by sputtering (typically a few tens of nm), followed by W CVD deposition.



• **CMP is used to planarize the wafer surface, completing the damascene process.**



• **Al is deposited on the wafer by sputtering. Mask #13 is used to pattern the Al and plasma etching is used to etch it.**



• **Intermetal dielectric and second level metal are deposited and defined in the same way as level #1. Mask #14 is used to define contact vias and Mask #15 is used to define metal 2. A final passivation layer of Si_3N_4 is deposited by PECVD and patterned with Mask #16.**

• **This completes the CMOS structure.**

Summary of Key Ideas

- This chapter serves as an introduction to CMOS technology.

- It provides a perspective on how individual technologies like oxidation and ion implantation are actually used.

- There are many variations on CMOS process flows used in industry.

- The process described here is intended to be representative, although it is simplified compared to many current process flows.

- Some process options are described in Chapter 2 in the text.

- Perhaps the most important point is that while individual process steps like oxidation and ion implantation are usually studied as isolated technologies, their actual use is very much complicated by the fact that IC manufacturing consists of many sequential steps, each of which must integrate together to make the whole process flow work in manufacturing.